MPT-500R/RH

Intelligent Railway Gateway System

User's Manual

Version 1.0
(October 2022)

iBASE

Disclaimer

IBASE reserves the right to make changes and improvements to the products described in this document without prior notice. Every effort has been made to ensure the information in the document is correct; however, IBASE does not guarantee this document is error-free. IBASE assumes no liability for incidental or consequential damages arising from misapplication or inability to use the product or the information contained herein, nor for any infringements of rights of third parties, which may result from its use.

Trademarks

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Compliance

CE

This product has passed CE tests for environmental specifications and limits in accordance with the directives of the Union European (EU). If users modify and/or install other devices in this equipment, the CE conformity declaration may no longer apply.

FC

This product has been tested and found to comply with the limits for a Class B device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the manufacturer's instructions, may cause harmful interference to radio communications.

WEEE

This product must not be disposed of as normal household waste, in accordance with the EU directive of for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

Green IBASE

This product is compliant with the current RoHS restrictions that prohibits the use of the following substances in concentrations exceeding 0.1% by weight (1000 ppm) except for cadmium, limited to 0.01% by weight (100 ppm).

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

Important Safety Information

Carefully read the precautions before using the device.

Environmental conditions:

- Lay the device horizontally on a stable and solid surface in case the device may fall, causing serious damage.
- Leave plenty of space around the device and do not block the openings for ventilation. NEVER DROP OR INSERT ANY OBJECTS OF ANY KIND INTO THE VENTIILATION OPENINGS.
- Slots and openings on the chassis are for ventilation. Do not block or cover these openings. Make sure you leave plenty of space around the device for ventilation.
- Use this product in environments with ambient temperatures between -40˚C and 70˚C for SSD, and between -25˚C and 55˚C for HDD.
- DO NOT LEAVE THIS DEVICE IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -40˚C OR ABOVE 85˚C. This could damage the device. The device must be used in a controlled environment.

Care for your IBASE products:

- Before cleaning the device, turn it off and unplug all cables such as power in case a small amount of electrical current may still flow.
- Use neutral cleaning agents or diluted alcohol to clean the device chassis with a cloth. Then wipe the chassis with a dry cloth.
- Vacuum the dust with a computer vacuum cleaner to prevent the air vent or slots from being clogged.

WARNING

Attention during use:

- Do not use this product near water.
- Do not spill water or any other liquids on your device.
- Do not place heavy objects on the top of the device.
- Operate this device from the type of power indicated on the marking label. If you are not sure of the type of power available, consult your distributor or local power company.
- If you use an extension cord, make sure that the total ampere rating of the product plugged into the extension cord does not exceed its limits.

Avoid Disassembly

You are not suggested to disassemble, repair or make any modification to the device. Disassembly, modification, or any attempt at repair could generate hazards and cause damage to the device, even bodily injury or property damage, and will void any warranty.

CAUTION

Danger of explosion if internal lithium-ion battery is replaced by an incorrect type. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Warranty Policy

- **IBASE standard products:**

  24-month (2-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

  12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by IBASE, such as CPU, memory, HDD, power adapter, panel and touchscreen.

* PRODUCTS, HOWEVER, THAT FAILS DUE TO MISUSE, ACCIDENT, IMPROPER INSTALLATION OR UNAUTHORIZED REPAIR SHALL BE TREATED AS OUT OF WARRANTY AND CUSTOMERS SHALL BE BILLED FOR REPAIR AND SHIPPING CHARGES.

Technical Support & Services

1. Visit the IBASE website at www.ibase.com.tw to find the latest information about the product.
2. If the product does not function properly, prepare the following information before contacting the distributor or sales representative:

   - Product model name
   - Product serial number
   - Detailed description of the problem
   - The error messages in text or in screenshots if there is any
   - The arrangement of the peripherals
   - Software in use (such as OS and application software, including the version numbers)

3. If repair service is required, you can download the RMA form at http://www.ibase.com.tw/english/Supports/RMAService/. Fill out the form and contact your distributor or sales representative.

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Table of Contents

Chapter 1
General Information

The information provided in this chapter includes:

- Features
- Packing List
- Specifications
- Product View
- Dimensions

1.1 Introduction

The MPT-500R is an embedded computer designed for railway applications. compliant. It is powered by Intel® Atom® Processor x6412RE (2-Core 6W 1.2GHz) or Intel® Atom® Processor x6425RE (4 Core 12W 1.9GHz) with robust M12 connectors and operating temperatures from ranging from -40°C and up to 70°C to provide reliable performance in high-speed, rugged environments.

MPT-500R

1.2 Features

- Onboard Intel® Atom™ x6412RE / x6425RE processor
- Onboard 4G/8G LPDDR4 memory
- Robust M12 connection for dual Gigabit Ethernet
- 3 x LAN Port: 1 x 2.5G + 2 x 1G with PoE (15.4W)
- Isolated USB, RS485, DIDO ports
- Dual SIM socket supports, 4G/5G
- Supports 1x M.2 2280 M key (PCIe M.2 SSD), 1x Mini-PCIe slot
- 24VDC (±30%) or 72V/110VDC main power input
- EN50155:2021 and EN45545-2 certification
- Quick-open chassis design

1.3 Packing List

Your product package should include the items listed below. If any of the items below is missing, contact the distributor or the dealer from whom you purchased the product.

Item	Q'ty	IBASE P/N
MPT-500R/RH	1	- -
Mounting Bracket	2	- -
Screw for Mounting Bracket 	4	H0230461012200A11P
Flat head screws for Mini PCIe / M.2 B-key, M.2 M-key cards 	3	H0220351112200A00P

1.4 Optional Accessories

IBASE provide optional accessories as follows. Please contact us or your dealer if you need any.

Item	IBASE P/N
Fuse for MPT-500R	C2309001151058000P
Fuse for MPT-500RH	C2313000501400100P
M12 Power Cable	C501PW39904121000P
M12 USB1.1/2.0 Cable	C501USB1320A32000P
M12 to RJ45 Cable	C501LAN6300A32000P
SSD;2.5" SATA3 64G MLC	A002SSDS3064G1000P
SSD;M.2-2280 GEN3.0 250G MLC	A002SSDM2S250G100P

1.5 Specifications

Product Name	MPT-500R	MPT-500RH	MPT-500RHA	MPT-500RE
Motherboard	MBT-501RX25	MBT-501RX25	MBT-501RX25A	MBT-501RX12
Intel® CPU*	x6425RE	x6425RE	x6425RE	x6412RE
	* Intel® Atom® Processor x6412RE - 2 Core 6W, 1.2GHz * Intel® Atom® Processor x6425RE - 4 Core 12W, 1.9 GHz			
LPDDR4 3200 Memory	4GB on board	4GB on board	8GB on board	4GB on board
Max. Memory	16GB			
Power Input	24VDC	72/110VDC	72/110VDC	24VDC
Graphics	Intel® HD graphics Gen. 7 with 4EU Supports DX 11, OGL 3.0, OCL 1.2, OGLES 2.0			
Front I/O	• 1x Recessed access tact-switch for system power • 4x light-pipe for four status LED • 1x USB type-C with DP (5Gbps) • 6x LED with each port for network status • 2x USB3.0 stack type-A (5Gbps) • 2x external accessible SIM socket • 3x M12 8-pin X-code for LAN (Two GbE LAN come with PoE and one 2.5G LAN) • 1x M12 4-pin A-code for USB 1.1 • 1x M12 4-pin A-code for USB 2.0 • 1x 3.5mm audio connector for line output 1x 3.5mm audio connector for MIC input • LED Indicators 1 x green LED for power status 1 x white LED for storage activity status 2 x orange-green LED, programmable			
Rear I/O	• 1 x M12 4-pin A code power input • 1 x DSUB9 for RS-232/485 • 1 x DSUB9 for 2 x RS485 isolated • 1 x HDMI (type A) • 1 x USB 3.0 (type A) (10Gbps) • 1 x DSUB15 for 4 x DO/4 x DI and ground • 1 x M3 with washer screw hole for ground connection • 2 x SMA antenna holes with cap			
Expansion Slot	• 1 x M.2 B 3042/52 key (4G/5G) (supports SIM1) • 1 x mPCIe full/half socket (PCIe, USB 2.0) (supports SIM2)			
Storage	• 1x 2280 M.2 M-key (PCI-E M.2 SSD) • 1x 2.5" device bay for SSD or HDD. Default 2.5" 64G SSD			
BIOS	AMI BIOS			

Mechanical	
Construction	Aluminum, black painting
Dimensions	240 (W) x 138 (D) x 98 (H) mm 9.4” (W) x 5.4” (D) x 3.7” (H)
Weight	Under 1.5Kgs
Antenna	6 x SMA antenna holes with cap
Environmental	
Humidity	10 ~ 95% @ 45°C, (non-condensing)
Temperature	Operating Temperature: ● SSD w/o PCIe Card: -40°C ~70°C (w/o fan & SSD), up to 85°C for 10 minutes ● SSD w/ PCIe Card: -40°C ~55°C (w/o fan & SSD), up to 70°C for 10 minutes ● HDD: -25°C ~55°C (w/o fan & HDD), up to 70°C for 10 minutes Storage Temperature: -40°C ~ 85°C
Acoustic	0dB (Fanless)
Shock	50 m/S2, 30 msec (EN 61373)
Vibration	Function: 1 m/S2, 5Hz ~ 150 Hz (EN 61373) Lifetime: 7.9 m/S2, 5Hz ~ 150 Hz (EN 61373)
Dimensions	210 x 138 x 99mm
Standards	
Regulation	RoHS 2.0 (2011/65/EU) / REACH (EC 1907/2006)
Certification	● EN 50155:2021 ● EN 50121-3-2:2015 ● CE (EN 62368 / EN55032 / EN55035)/ FCC Class A ● EN45545-2
Operating System	● Windows 10 ● Linux kernel 3.8.0 or above (64 bits)

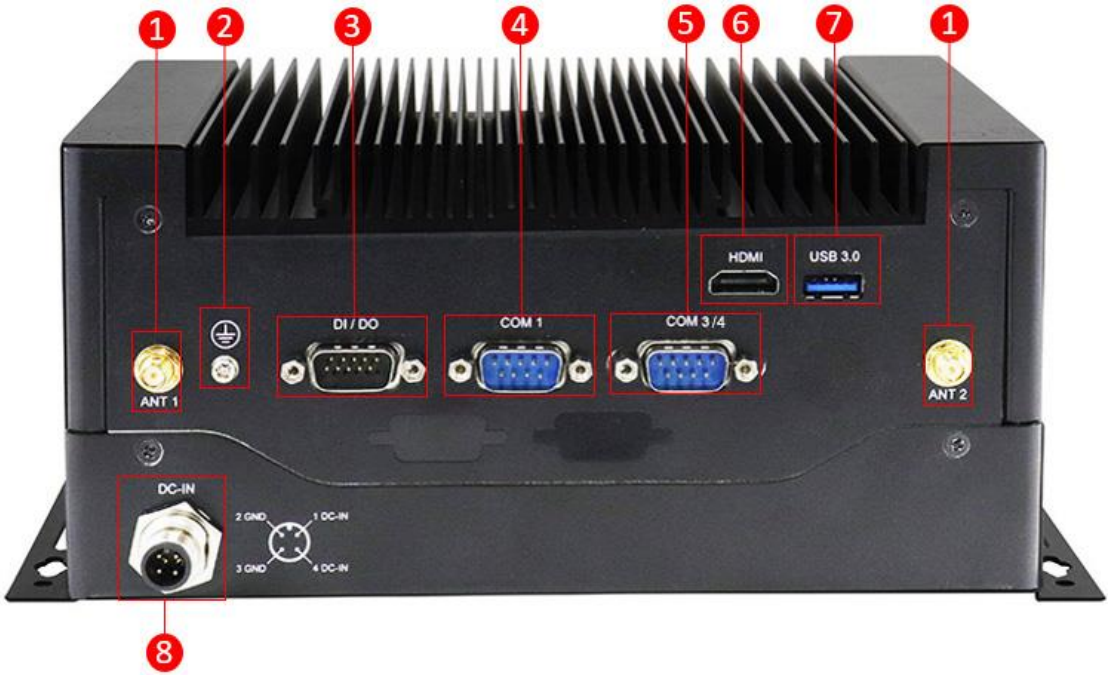
All specifications are subject to change without prior notice.

1.6 Product View

Front View

No.	Name	No.	Name
1	Power On/Off Button	6	LAN Ports (M12) (2x GbE with PoE and 1x 2.5G at LAN1)
2	4x LEDs for PWR/HDD/ Programmable(2x)	7	USB 1.1 / 2.0 Ports (M12)
3	USB type-C with DP (5Gbps)	8	USB 3.0 Ports
4	6x LEDs for network status	9	Line Out / Mic Jacks
5	Dual-SIM socket (with cover)		

Rear View



No.	Name	No.	Name
1	Antenna holes	5	DSUB15 for COM3/4 (2xRS485)
2	M3 screw for ground	6	HDMI port
3	DSUB15 for 4x DO /4x DI	7	USB 3.0 ports
4	DSUB15 for COM1 (RS232/485)	8	DC-in connector

Oblique View

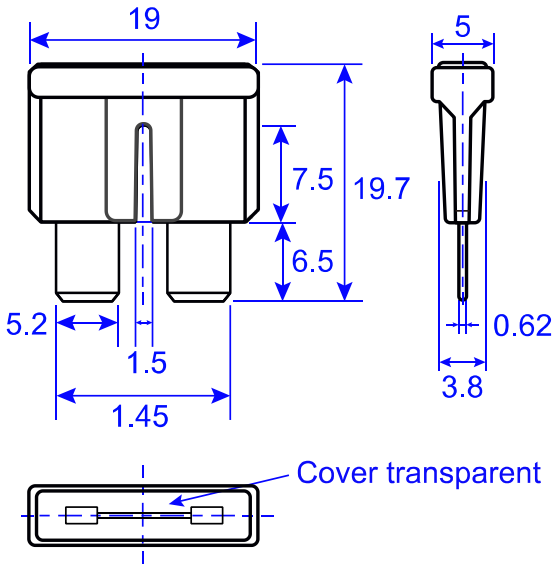
The oblique view also shows four (4) antenna connectors on the right side.

1.7 Fuse Dimensions

Unit: mm

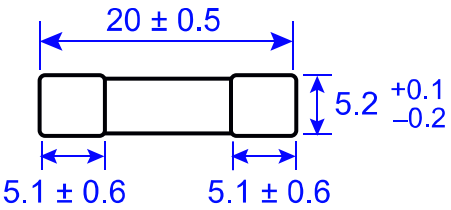
Fuse for MPT-500R:

Littlefuse® TAC ATO® Style Blade
15A, 58V DC



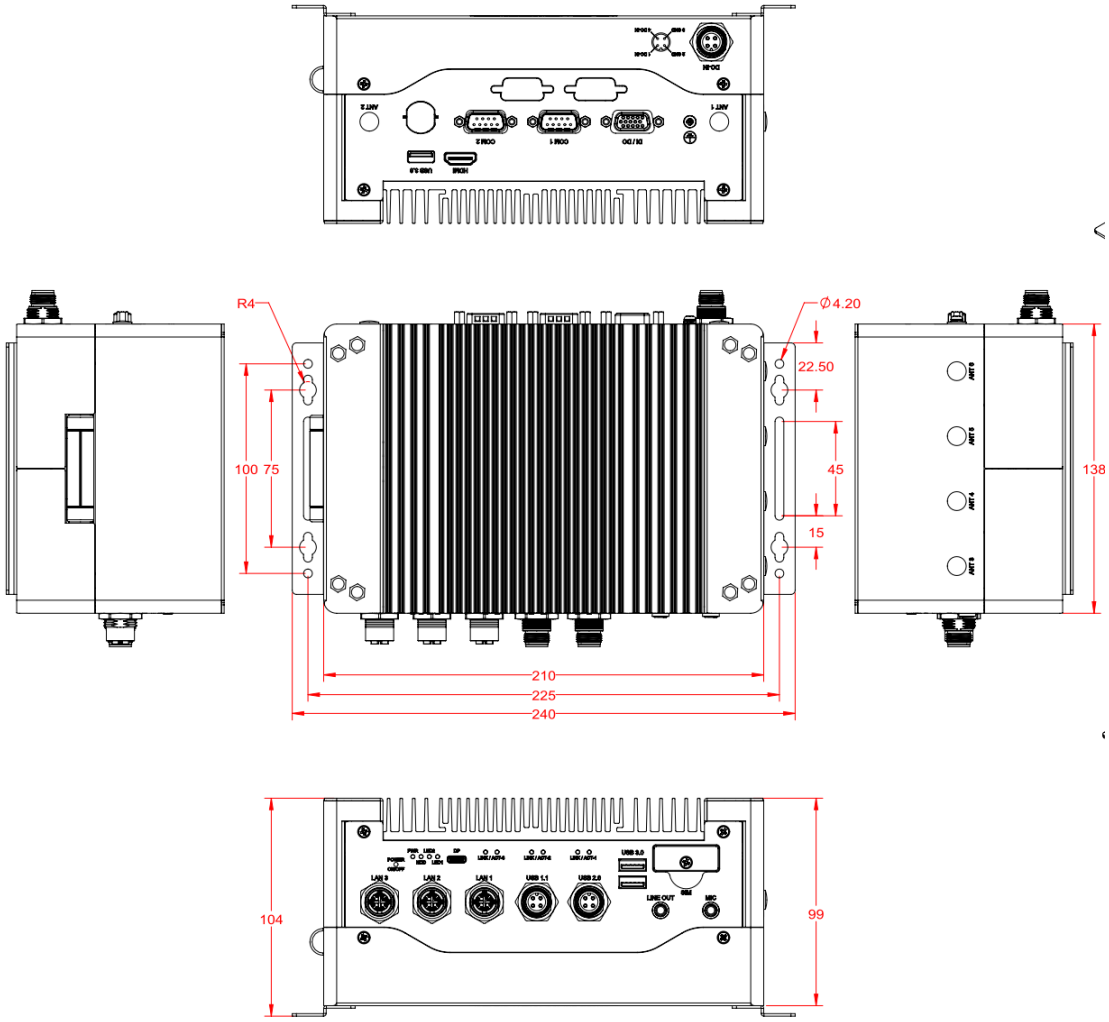
Fuse for MPT-500RH

Littelfuse® Time-lag Fuse
477 series 5A, 400V DC



1.8 Dimensions

Unit: mm



Chapter 2
Hardware Configuration

The information provided in this chapter includes:

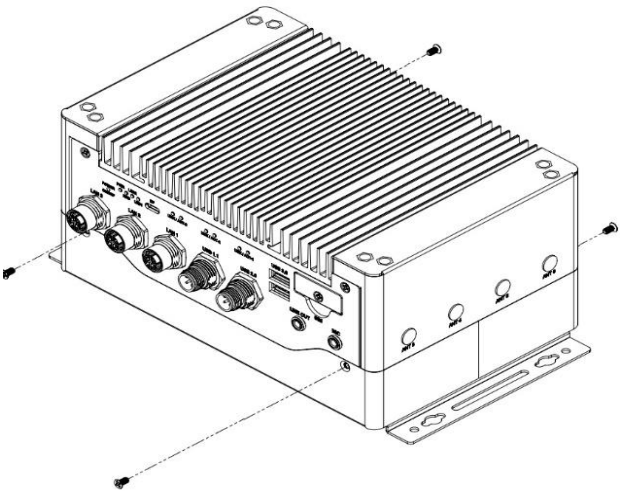
- Essential installations
- Switches, Jumpers & Connectors

2.1 Essential Installations

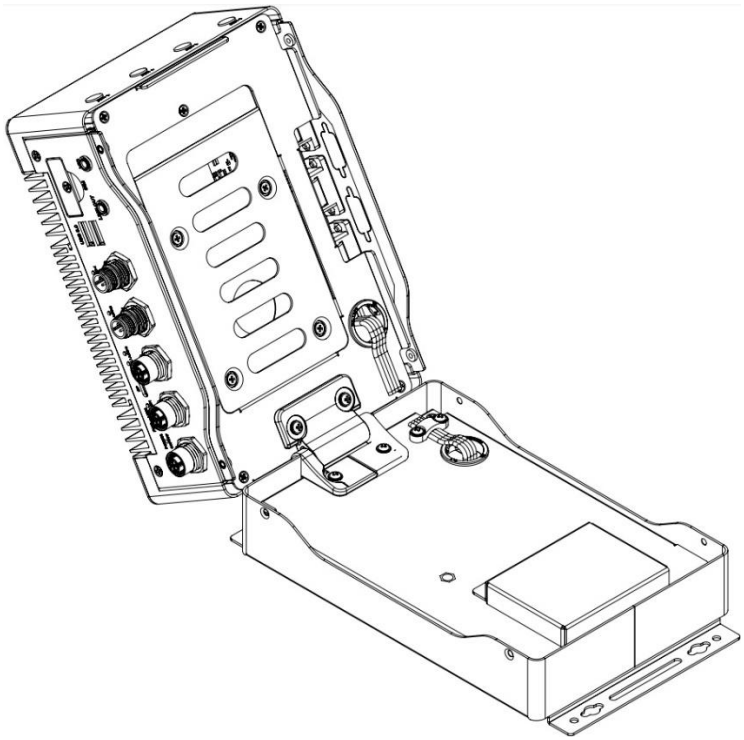
2.1.1 Installation of 2.5” SSD/HDD Storage

You can use either HDD, SSD or M.2 SATA card, or use both for storage. For HDD or SSD drive replacement or installation, follow the instructions below. For M.2 SATA card (M-keyed), it is discussed in the section 2.1.2.

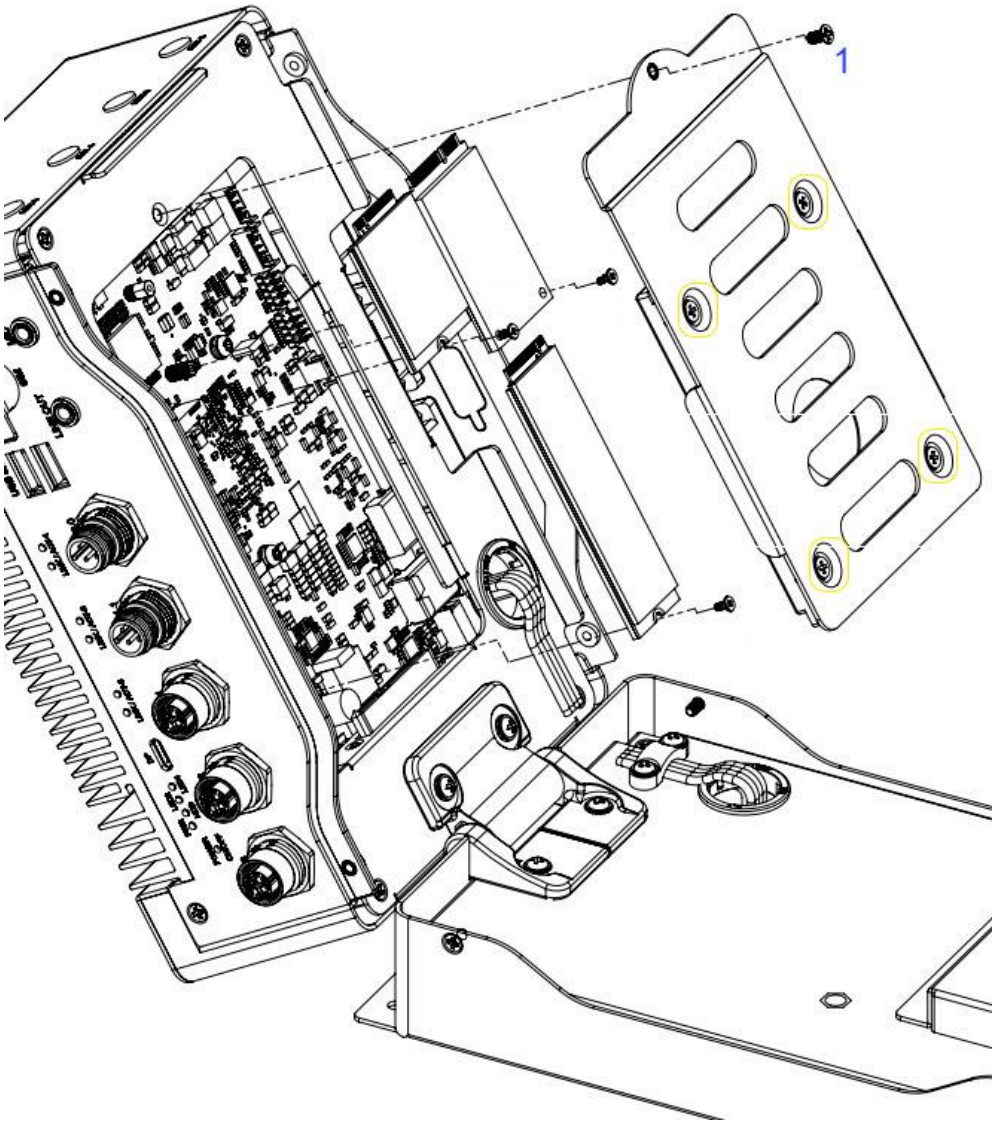
1. Release the four screws shown below.



2. Raise the top part of the system to an angle of 120 degrees.

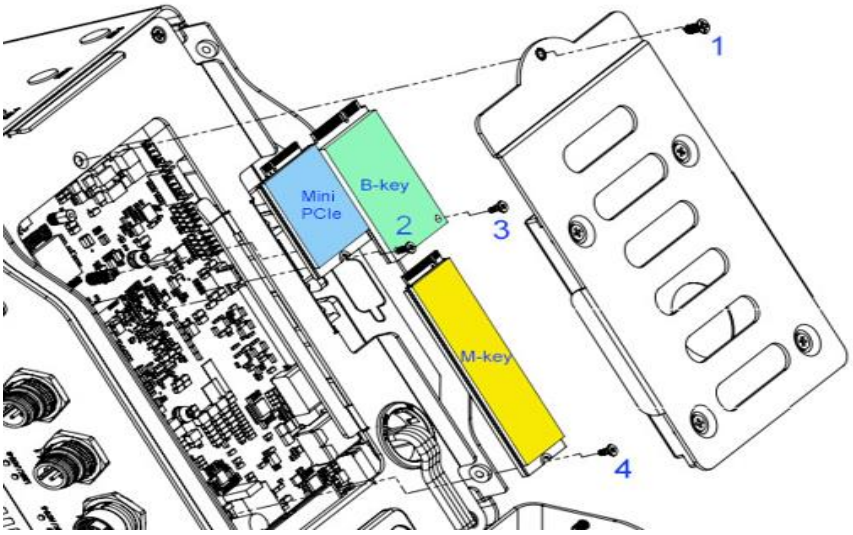


3. The internal components are covered by the 2.5” SSD/HDD tray or drive holder. Remove the single screw (1) to remove the storage holder. Continue to remove the four screws securing the SSD/HDD device to replace or remove it.

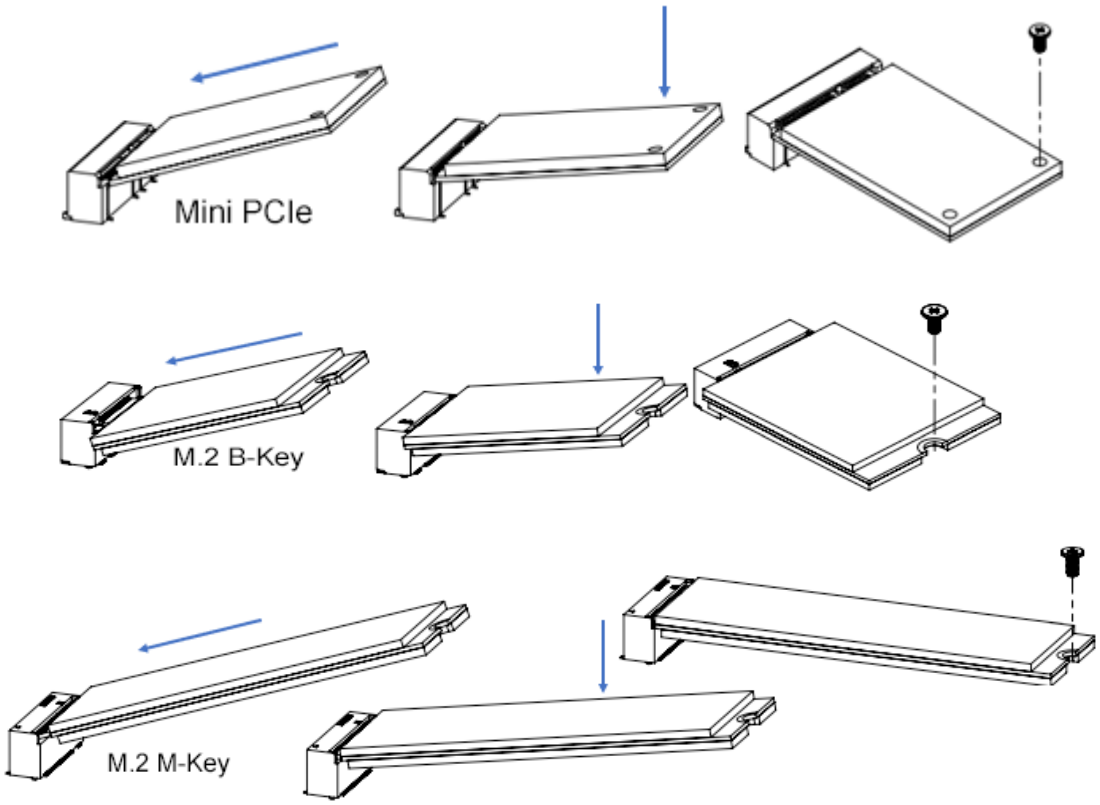


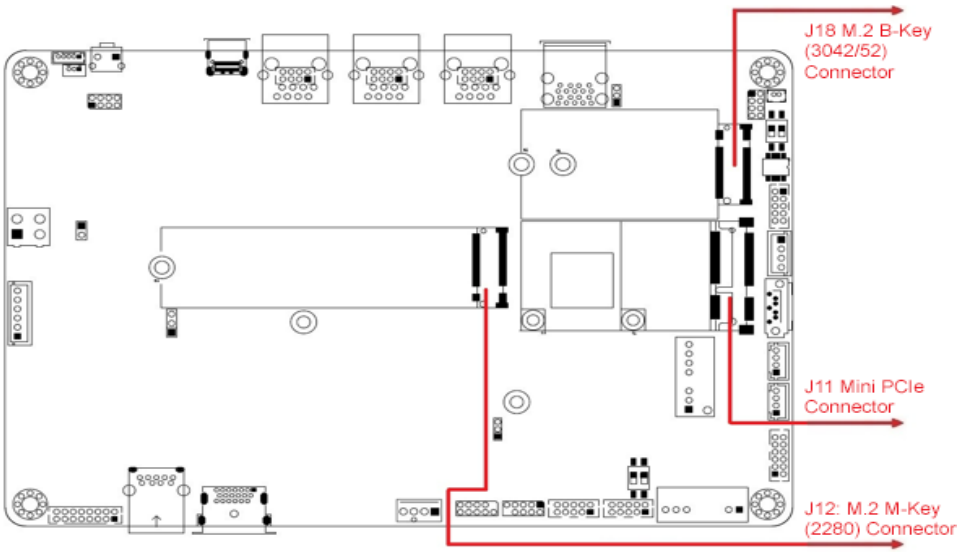
2.1.2 Installation for M.2 and Mini PCIe Cards

1. There are **three (3) sockets** that are accessible after removing the SSD/HDD holder (screw 1) – **Mini PCIe, M.2 B-key and M.2 M-key**.



2. To install or replace a card, locate the slot, align the key of the card to the interface, and insert the card slantwise.
3. Push the card down and fix it with the supplied flat head screw (P/N H0220351112200A00P).

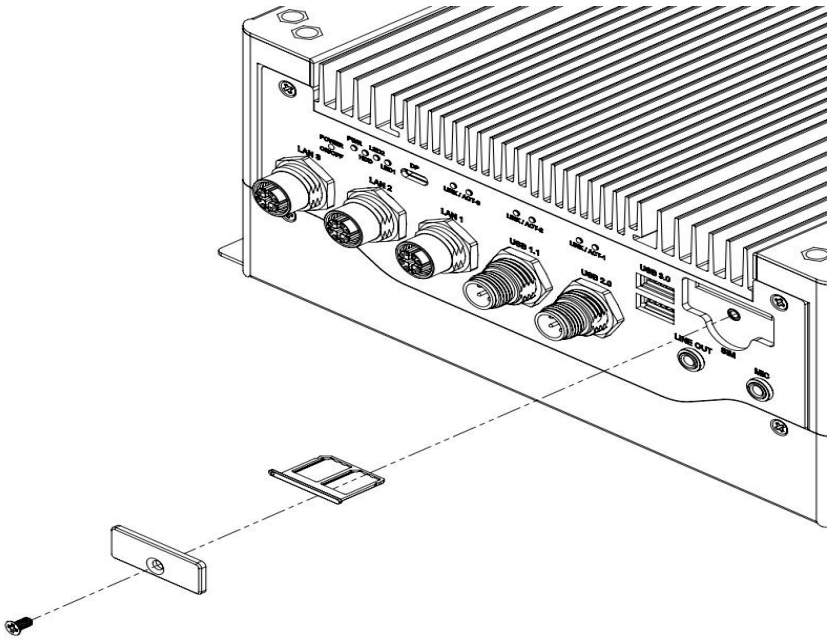




The above shows the positions of the M.2 and MPCIe slots on the board.

2.1.3 Nano SIM Card Installation

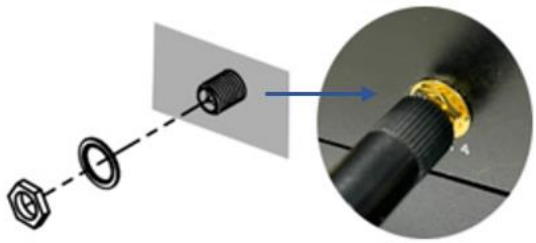
1. The SIM card slot is accessible externally and is secured by a single screw. Release the cover by removing the screw as shown below.
2. Push the card holder to release it. Insert the card holder back to its position and push it again to lock it into place. Replace the cover and screw it securely.



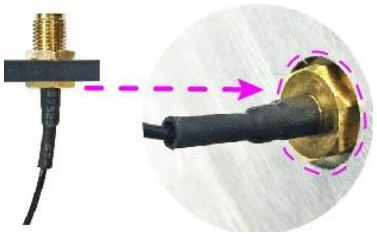
2.1.4 Antenna Installation

Thread the antenna extension cable through the antenna connectors in the system. There are a total of six antenna connectors, with two in front and four on the side. Fasten the antenna as shown below and apply adhesive to the edge of the hex nut to prevent the extension cable from falling off.

1. Thread and fasten the hex nut and the washer. Then install the antenna.



2. Apply adhesive around here.

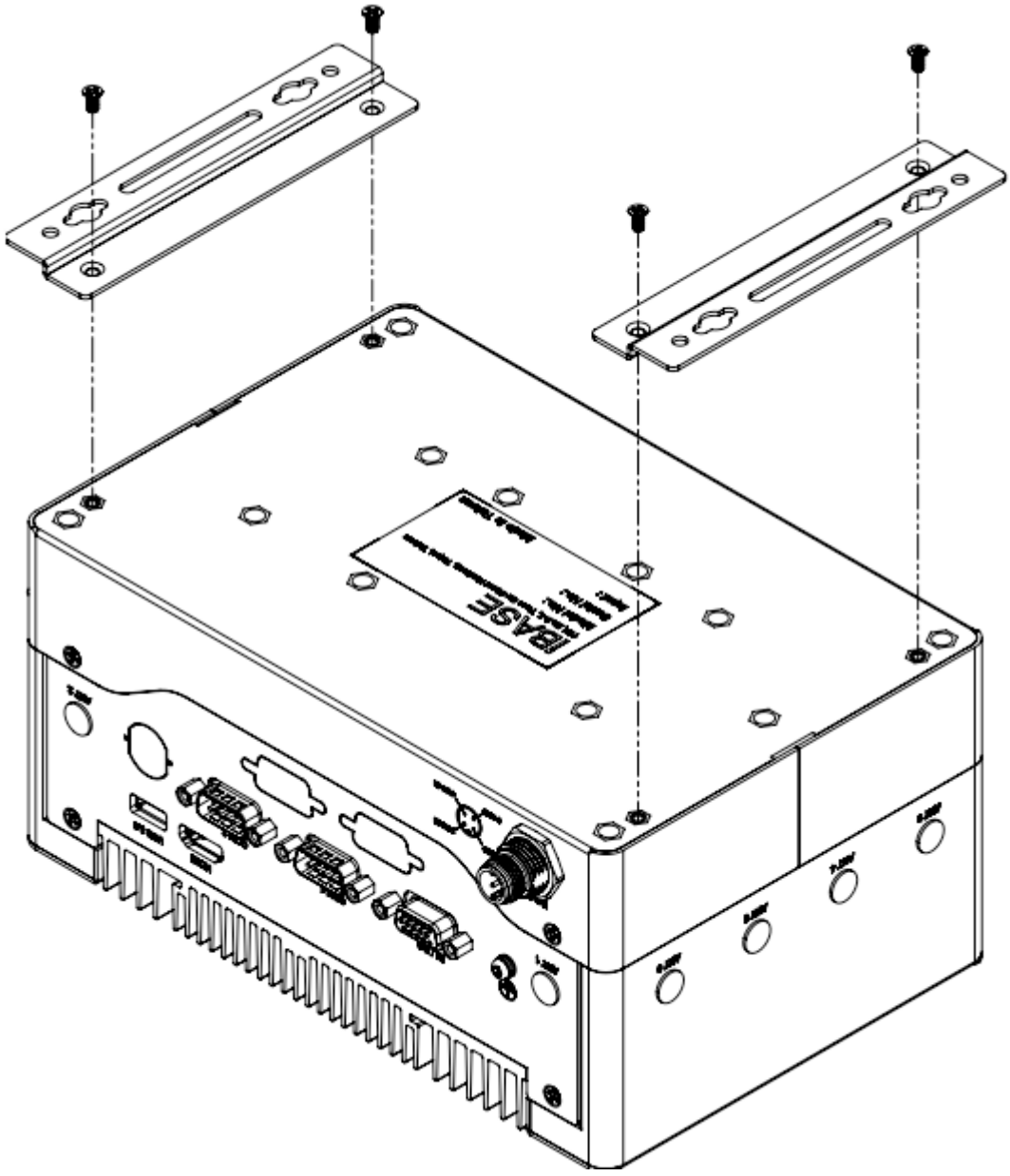


Info: The diameter of the nut is around 6.35 mm (0.25”-36UNC).

There are a total of six (6) antennas in the system.

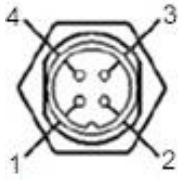
2.1.5 Mounting Brackets Installation

1. Turn your MPT-500R upside down to attach the mounting brackets and secure the brackets with the supplied screws (P/N H0230461012200A11P) as shown below.



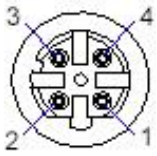
2.1.6 Pinout for M12 Connectors (Power Input, USB 2.0, LAN, COM)

- **Power Input (M12, 4-pin, male A-coded)**



Pin	Assigment	Pin	Assigment
1	DC-Input	3	Ground
2	Ground	4	DC-Input

- **USB 1.1/2.0 Port (M12, 4-pin female A-code)**



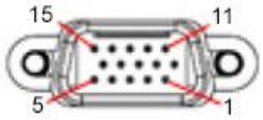
Pin	Assigment	Pin	Assigment
1	Vcc (+5V)	3	Data +
2	Data -	4	Ground-

- **COM1 Connector**

Pin	Signal Name	
	RS-232	RS-485
1	DCD	DATA-
2	RX	DATA+
3	TX	NC
4	DTR	NC
5	Ground	Ground
6	DSR	NC
7	RTS	NC
8	CTS	NC

9	RI	NC

- **Digital I/O Connector**



Pin	Assignment	Pin	Assignment
1	DO0	6	DI0
2	DO1	7	DI1
3	DO2	8	DI2
4	DO3	9	DI3
5	NC	10	Ground

- **COM3 / COM4 Connector**

Pin	Assignment	Pin	Assignment
1	NC	6	COM4(D+)
2	NC	7	COM3(D+)
3	Ground	8	COM4(D-)
4	Ground	9	Ground
5	COM3(D-)	10	Ground

- **LAN Port (M12, 8-pin, female X-coded)**

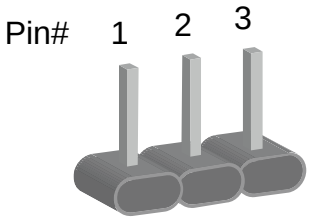
Pin	Assigment	Pin	Assigment
1	MX1+	5	MX2-
2	MX3-	6	MX4+
3	MX3+	7	MX1-
4	MX4-	8	MX2+

2.2 Setting the Jumpers

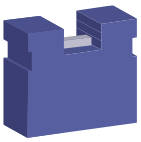
Set up and configure your MPT-500R by using jumpers for various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your use.

2.2.1 How to Set Jumpers

Jumpers are short-length conductors consisting of several metal pins with a non-conductive base mounted on the circuit board. Jumper caps are used to have the functions and features enabled or disabled. If a jumper has 3 pins, you can connect either PIN1 to PIN2 or PIN2 to PIN3 by shorting.

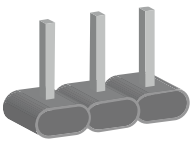
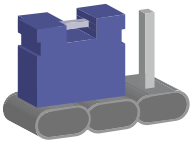
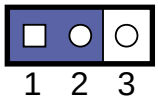
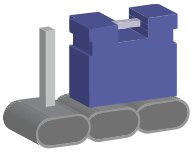
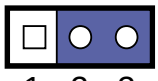


A 3-pin jumper



A jumper cap

Refer to the illustration below to set jumpers.

Pin	Oblique view	Illustration
Open		
1-2 closed		
2-3 closed		

When two pins of a jumper are encased in a jumper cap, this jumper is **closed**, i.e. turned **On**.

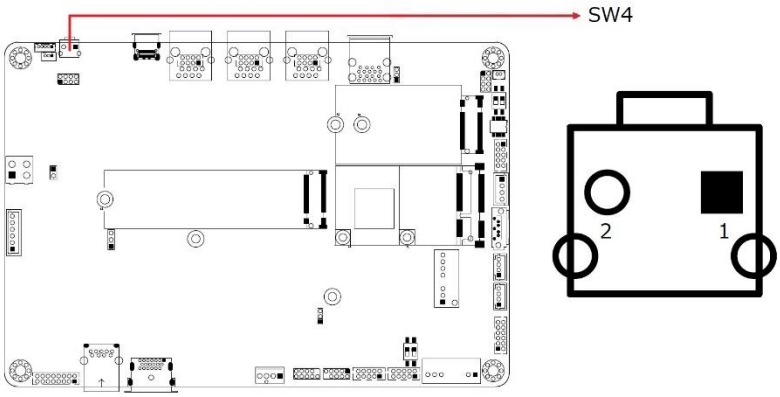
When a jumper cap is removed from two jumper pins, this jumper is **open**, i.e. turned **Off**.

2.3 Switches, Jumpers & Connectors Locations

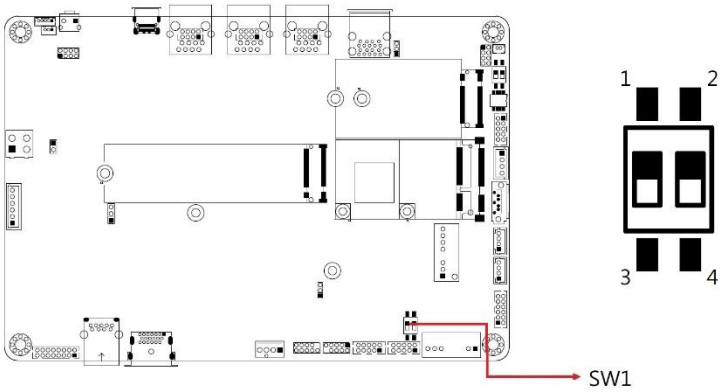
Here is a list of the switches, jumpers and connectors in the system.

2.4 Switches and Jumpers

2.4.1 SW4: Power Button



2.4.2 SW1_1: COM3 RS-485 Terminal Register

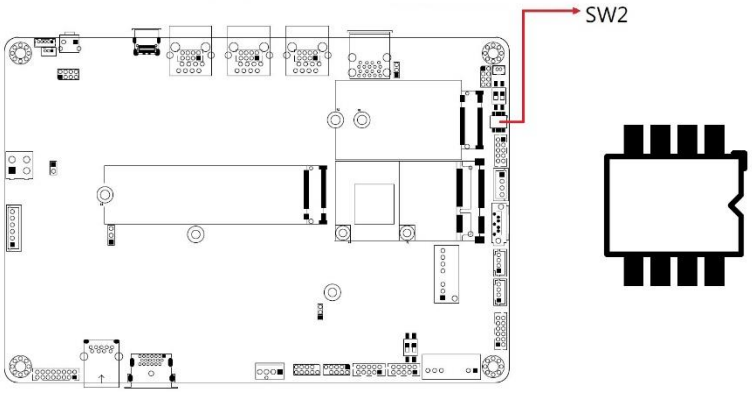


Setting	Function
Pin_1 Off	COM3 Terminal Disable (Default)
Pin_1 On	COM3 Terminal Enable

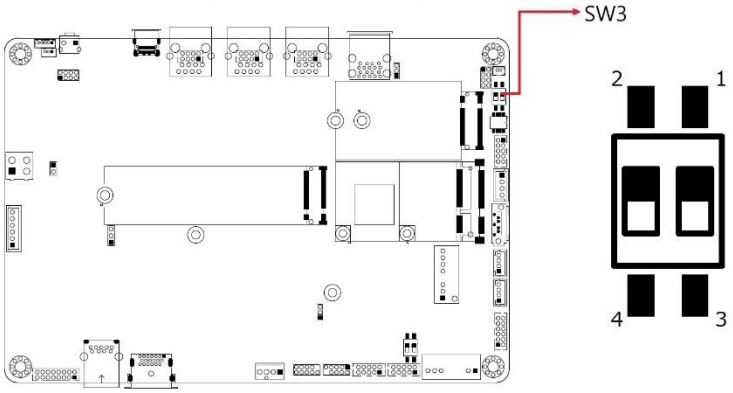
2.4.3 SW1_2: COM4 RS-485 Terminal Register

Setting	Function
Pin_2 Off	COM4 Terminal Disable (Default)
Pin_2 On	COM4 Terminal Enable

2.4.4 SW2: Digital I/O test (Factory use only)



2.4.5 SW3_1: Clear CMOS Data

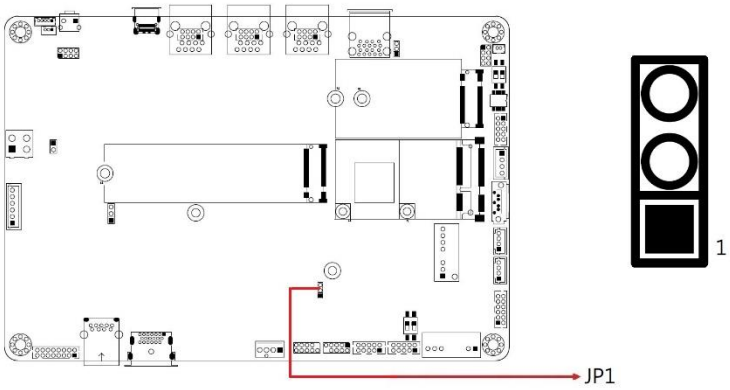


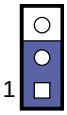
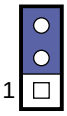
Setting	Function
Pin_1 Off	Normal (Default)
Pin_1 On	Clear CMOS

2.4.6 SW3_2: Clear ME Register

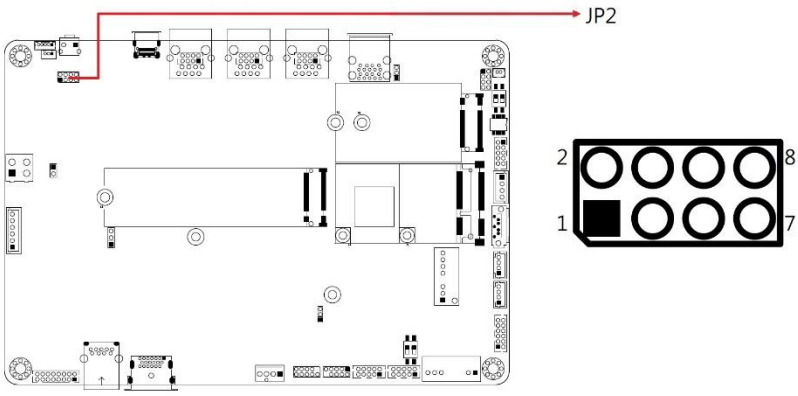
Setting	Function
Pin_2 Off	Normal (Default)
Pin_2 On	Clear ME

2.4.7 JP1: AT/ATX Mode Selection



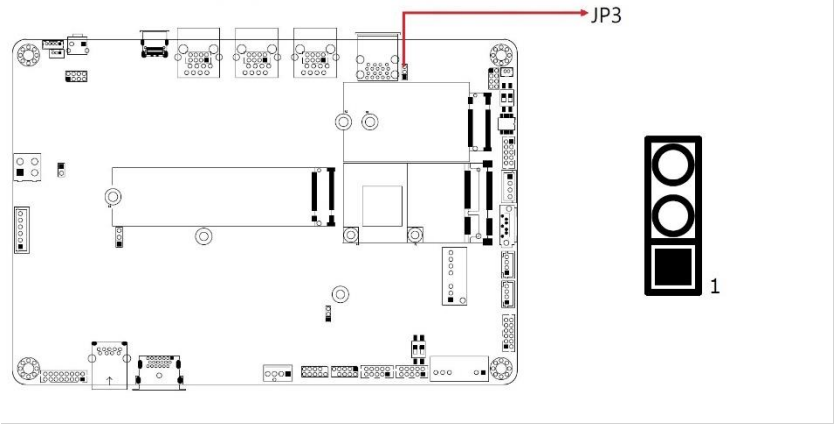
Function	Pin closed	Illustration
ATX (default)	1-2	
AT	2-3	

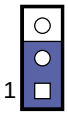
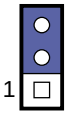
2.4.8 JP2: POE Mode Setup (Factory use only)



Pin	Assigment	Pin	Assigment
1	4266_AUTO	5	Vcc
2	4266_MID	6	Vcc
3	4266_RESET	7	Ground
4	4266_MSD	8	Ground

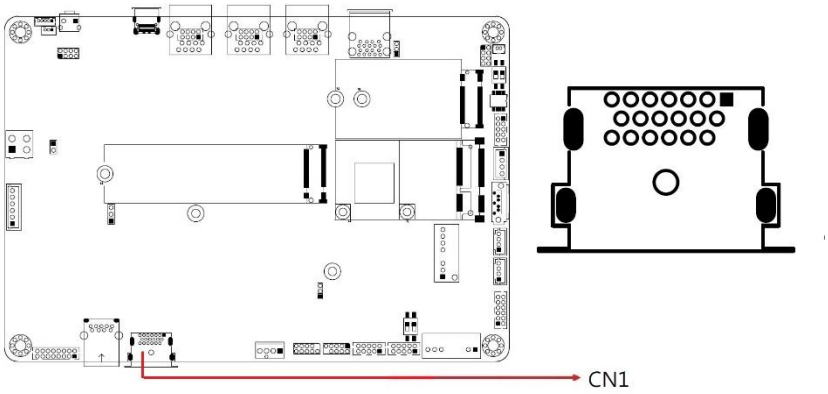
2.4.9 JP3: Sierra 5G Wireless Card USB/PCIE I/F Selection



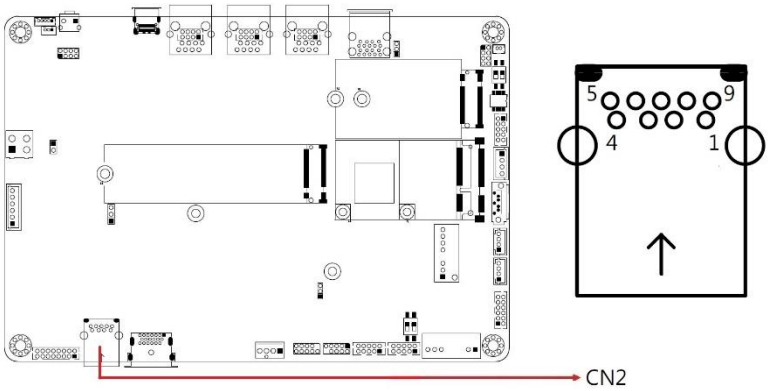
USB (Default)	1-2	
PCIE	2-3	

2.5 Connectors

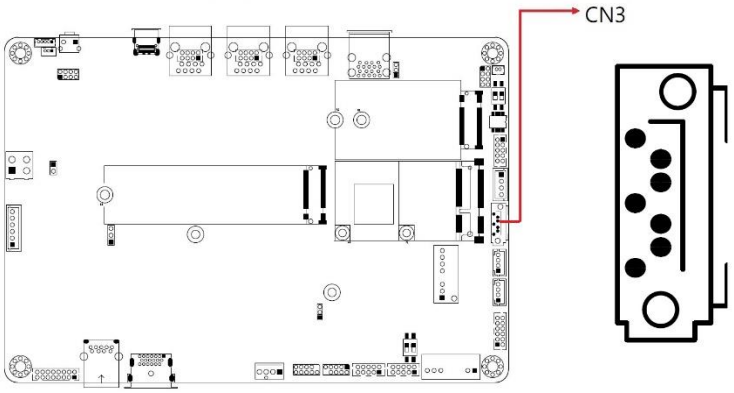
2.5.1 CN1: HDMI Connector



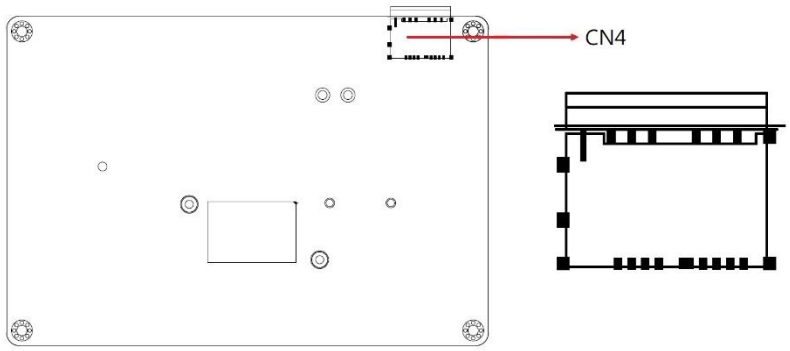
2.5.2 CN2: USB3 Type A Connector (supports USB3 Gen2)



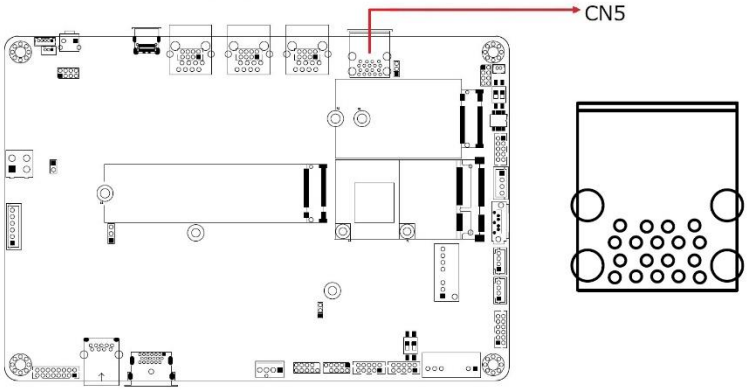
2.5.3 CN3: SATA Connector



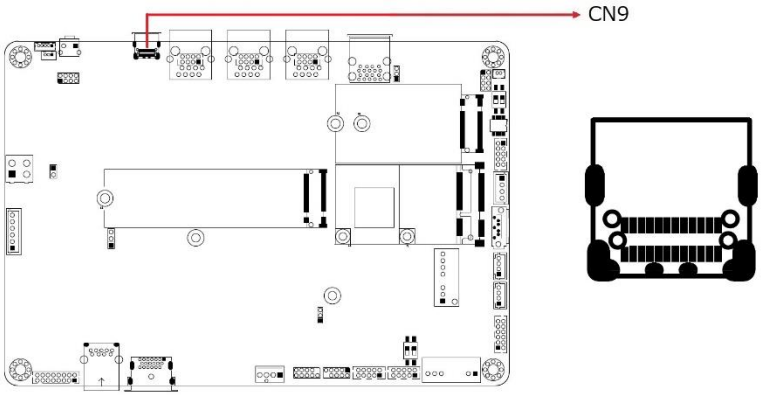
2.5.4 CN4: Nano SIM Card Connector



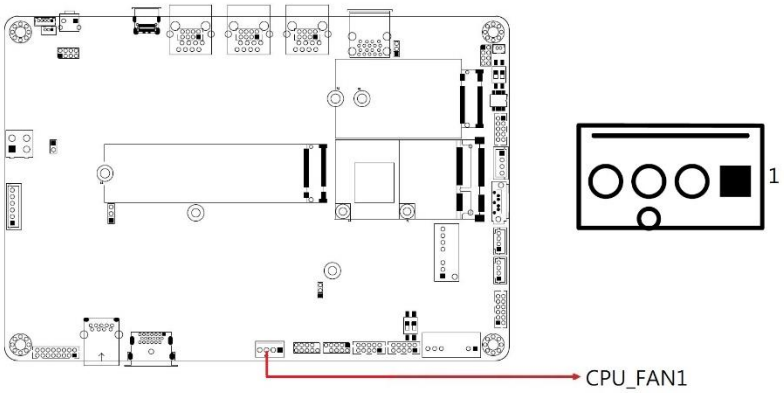
2.5.5 CN5: USB3 Type A Connector (supports USB3 Gen1)



2.5.6 CN9: Type C Connector (supports USB3 Gen1)

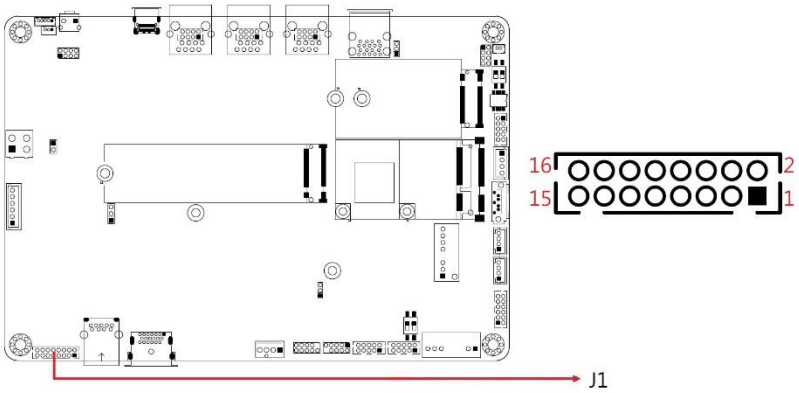


2.5.7 CPU_FAN1: CPU Fan Power Connector



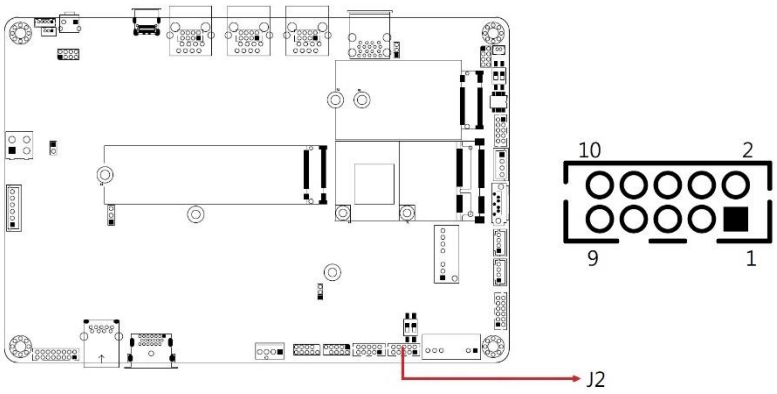
Pin	Assigment
1	Ground
2	+12V
3	Rotation detection
4	Control

2.5.8 J1: VGA Connector (HRS_DF11-16DP-2DSA(08))



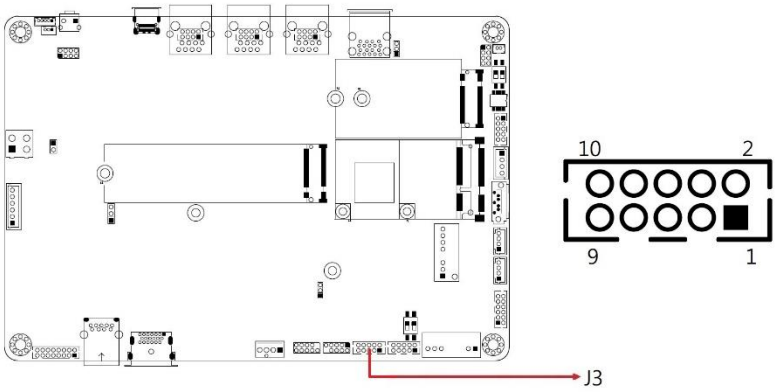
Pin	Signal Name	Pin	Signal Name
1	CRT_R	2	+5V
3	CRT_G	4	GND
5	CRT_B	6	NC
7	NC	8	DDC_DATA
9	GND	10	CRT_HSYN
11	GND	12	CRT_VSYN
13	GND	14	DDC_CLK
15	GND	16	NC

2.5.9 J2: COM3,4 RS-485 Connector (HK_DF11-10S-PA66H)



Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	GND	4	GND
5	RS485-DATA3-	6	RS485-DATA4-
7	RS485-DATA3+	8	RS485-DATA4+
9	GND	10	GND

2.5.10 J3: COM1 Connector (HK_DF11-10S-PA66H)

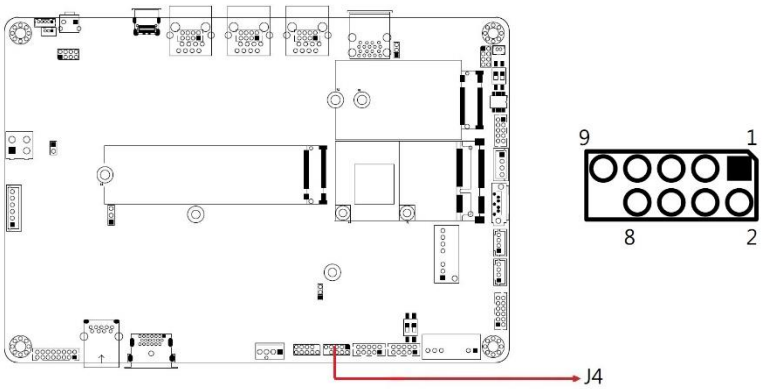


Pin	Signal Name	Pin	Signal Name
1	DCD, Data carrier detect	2	RXD, Receive data
3	TXD, Transmit data	4	DTR, Data terminal ready
5	GND, ground	6	DSR, Data set ready
7	RTS, Request to send	8	CTS, Clear to send
9	RI, Ring indicator	10	Not Used

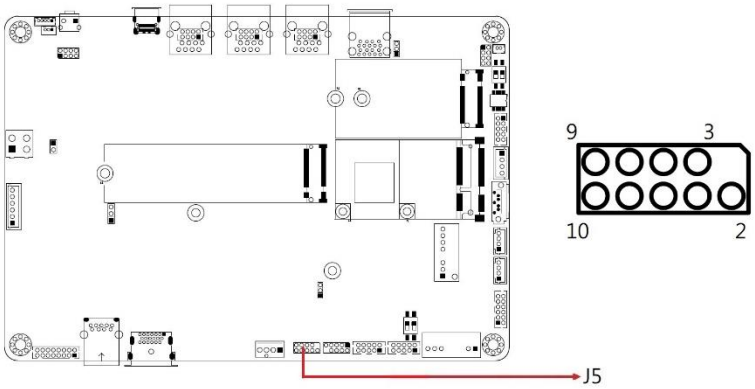
COM1 is jumper-less for RS-232, RS-422 and RS-485 and configured with BIOS Selection.

Pin	Signal Name		
	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

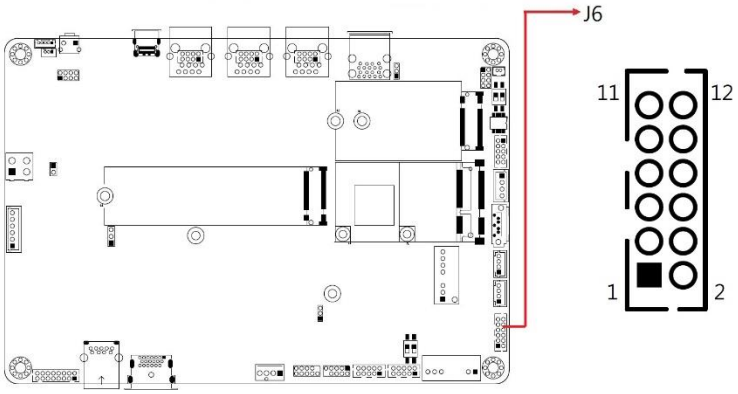
2.5.11 J4: ESPI Debug 80 Port (Factory use only)



2.5.12 J5: SPI ROM Flash Connector (Factory use only)

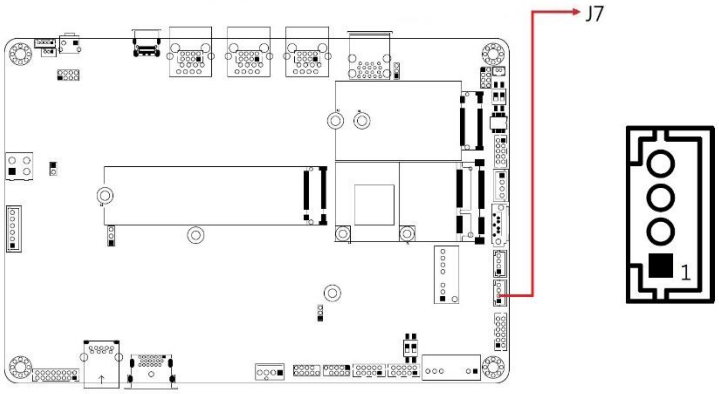


2.5.13 J6: Audio Connector (HK_DF11-12S-PA66H)



Pin	Signal Name	Pin	Signal Name
2	LINEOUT_R	1	LINEOUT_L
4	Ground	3	JD_FRONT
6	NC	5	NC
8	NC	7	NC
10	MIC-R	9	MIC_L
12	Ground	11	JD_MIC1

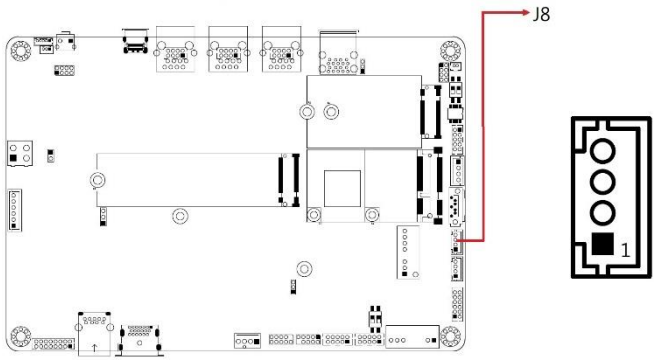
2.5.14 J7: USB_2.0 Connector (E-Call_0110-161-040)



Pin	Assigment
1	VCC
2	D-
3	D+
4	Ground

Note: USB Enable/Disable Selection by BIOS

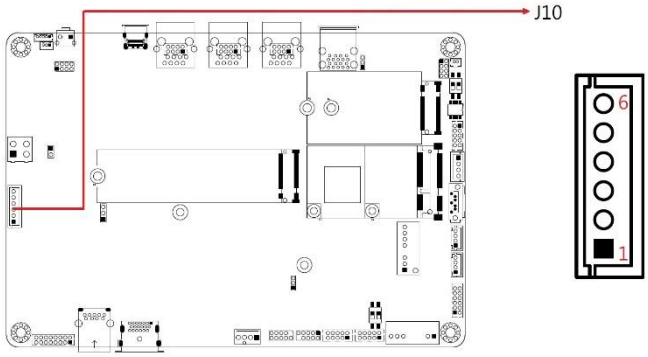
2.5.15 J8: USB_1.1 Connector (E-Call_0110-161-040)



Pin	Assigment
1	VCC
2	D-
3	D+
4	Ground

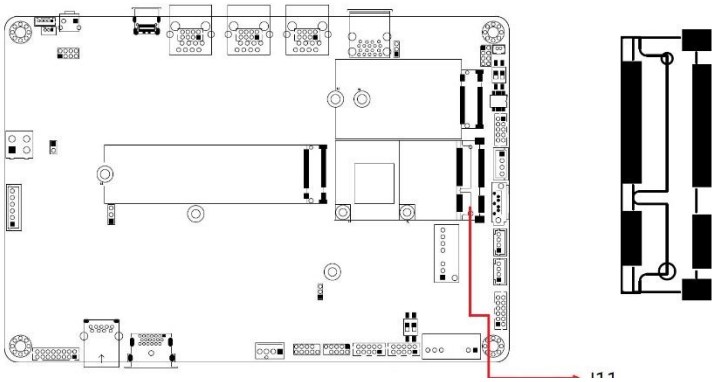
Note: USB Enable/Disable Selection by BIOS

2.5.16 J10: External Super CAP Connector (E-Call_0110-071-060)

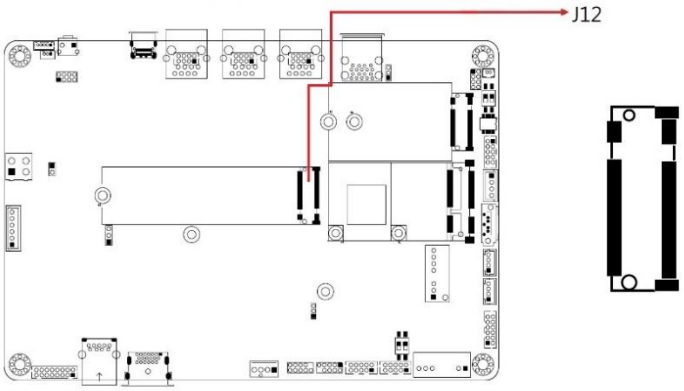


Pin	Assigment
1	+12VDUAL
2	+12VDUAL
3	+12VDUAL
4	Ground
5	Ground
6	Ground

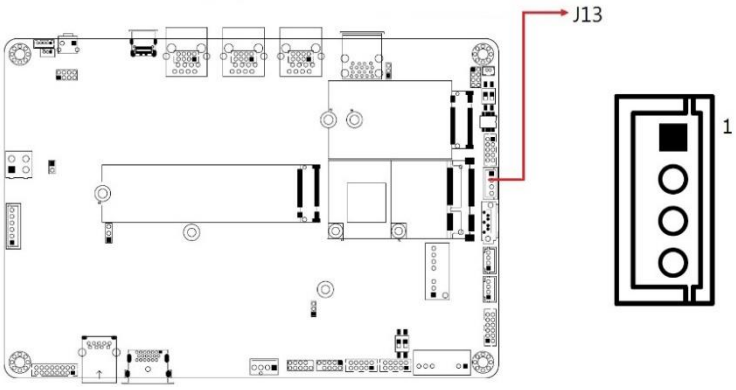
2.5.17 J11: Mini PCIE Connector with PCIe (x1), USB 2.0, SIM Card



2.5.18 J12: M.2 M-Key (2280) Connector with PCIe (x1)

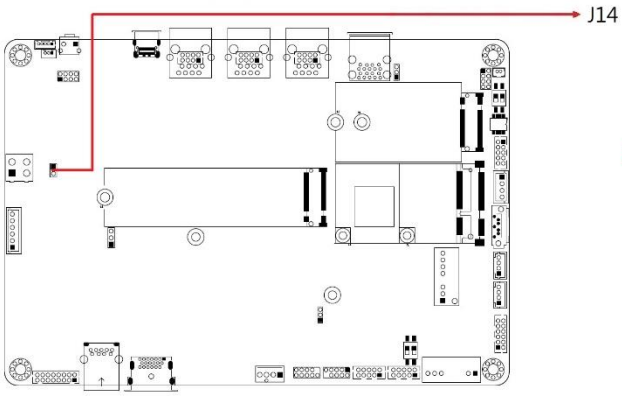


2.5.19 J13: SATA HDD Power Connector (E-Call_0110-071-040)

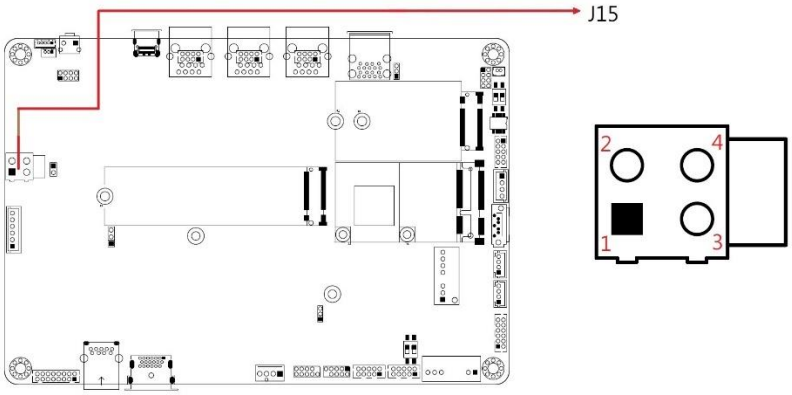


Pin	Assigment
1	+5V
2	Ground
3	Ground
4	+12V

2.5.20 J14: POE Debug Setting (Factory use only)

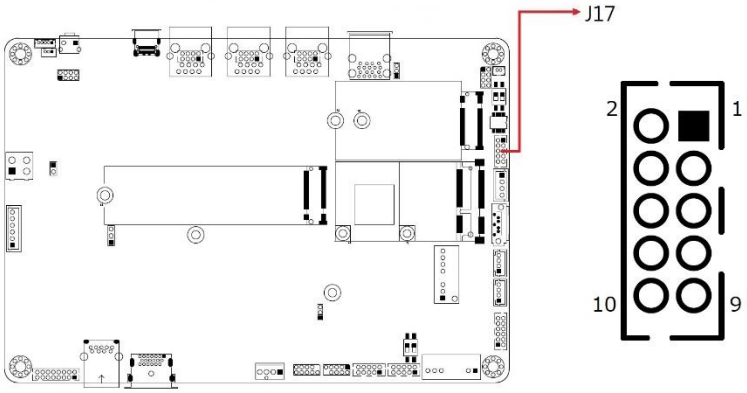


2.5.21 J15: DC_IN 12V Power Connector (HK_ATX4PT-NY46)



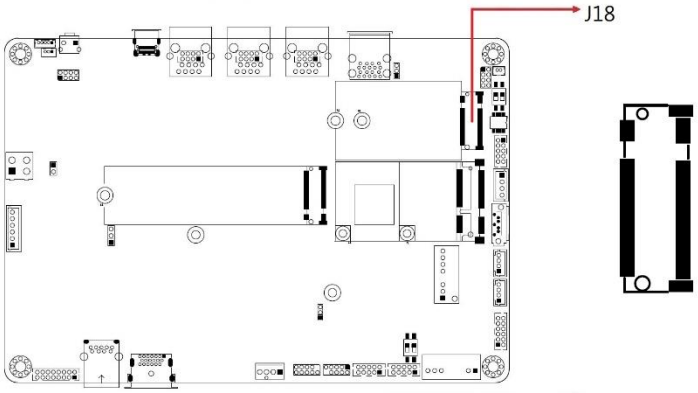
Pin	Signal Name	Pin	Signal Name
3	+12V	1	Ground
4	+12V	2	Ground

2.5.22 J17: Digital I/O Connector (HK_DF11-10S-PA66H)

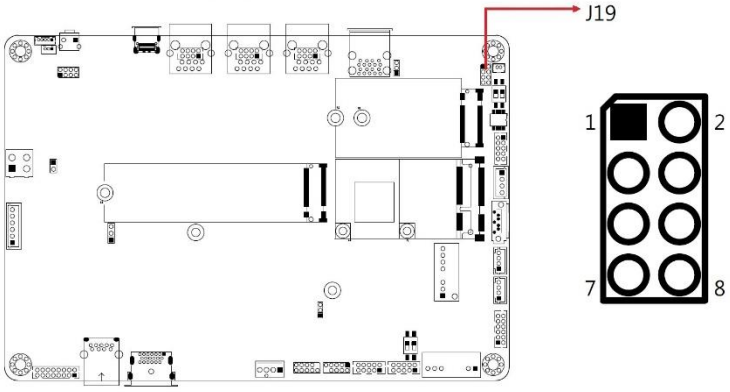


Pin	Signal Name	Pin	Signal Name
1	OUT0	2	IN0
3	OUT1	4	IN1
5	OUT2	6	IN2
7	OUT3	8	IN3
9	Power	10	Ground

2.5.23 J18: M.2 B-Key (3042/52) Connector with PCIe (x1), USB 2.0, USB 3.0, SIM Card



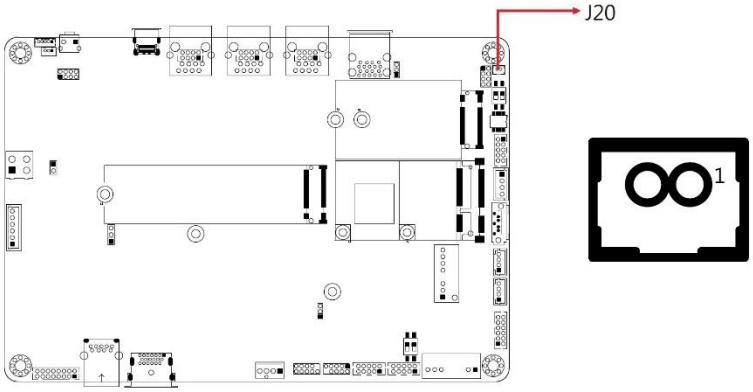
J19: System Function Connectors (E-Call_0196-01-200-080)



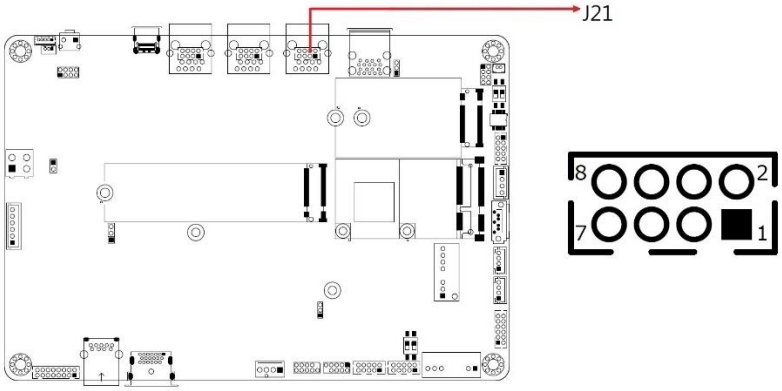
J19 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. J19 is an 8-pin header that provides interfaces for the following functions:

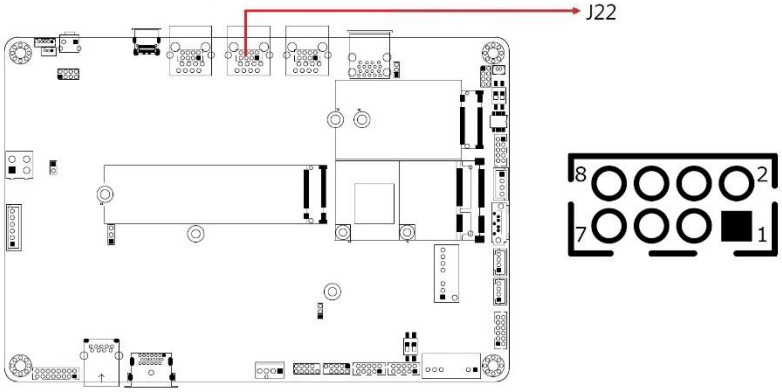
Pin	Signal Name	Pin	Signal Name
1	Power BTN-	2	Power BTN+
3	HDD LED+	4	HDD LED-
5	Ground	6	Reset BTN+
7	Power LED+	8	Ground

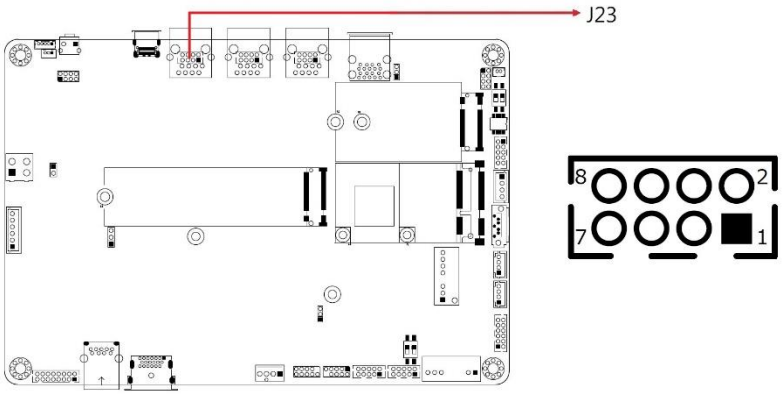
2.5.24 J20: Battery Connector (Molex_53047-0210)



2.5.25 J21, J22, J23: LAN1,2,3 Connector (HRS_DF11-8DP-2DSA(08))

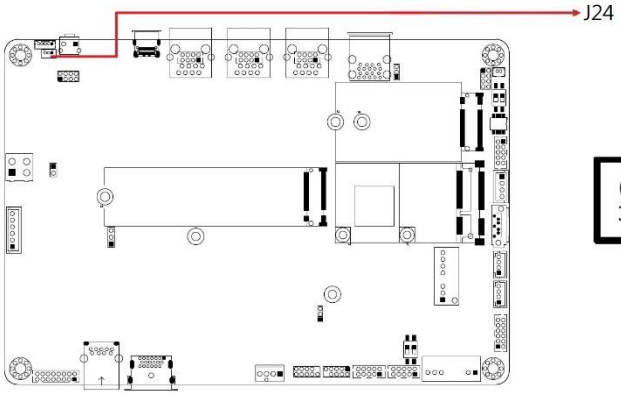


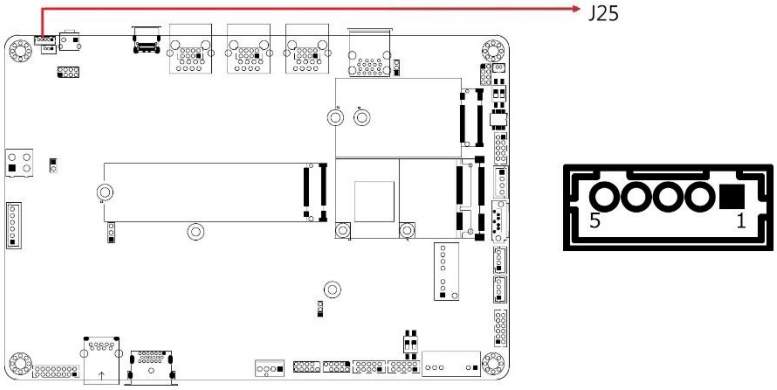




Pin	Signal Name	Pin	Signal Name
1	MDI_P0	2	MDI_N0
3	MDI_P1	4	MDI_N1
5	MDI_N2	6	MDI_P2
7	MDI_P3	8	MDI_N3

2.5.26 J24, J25: USB Type C Flash Connector (Factory use only)





Chapter 3
Driver Installation

The information provided in this chapter includes:

- Intel® Chipset Software Installation Utility
- VGA Driver Installation
- HD Audio Driver Installation
- Intel® ME Drivers Installation
- LAN Driver Installation

3.1 Introduction

This section describes the installation procedures for software drivers. The software drivers are in a disk enclosed with the product package. If you find anything missing, please contact the distributor where you made the purchase.

Note: After installing your Windows operating system, you must install the Intel® Chipset Software Installation Utility first before proceeding with the drivers installation.

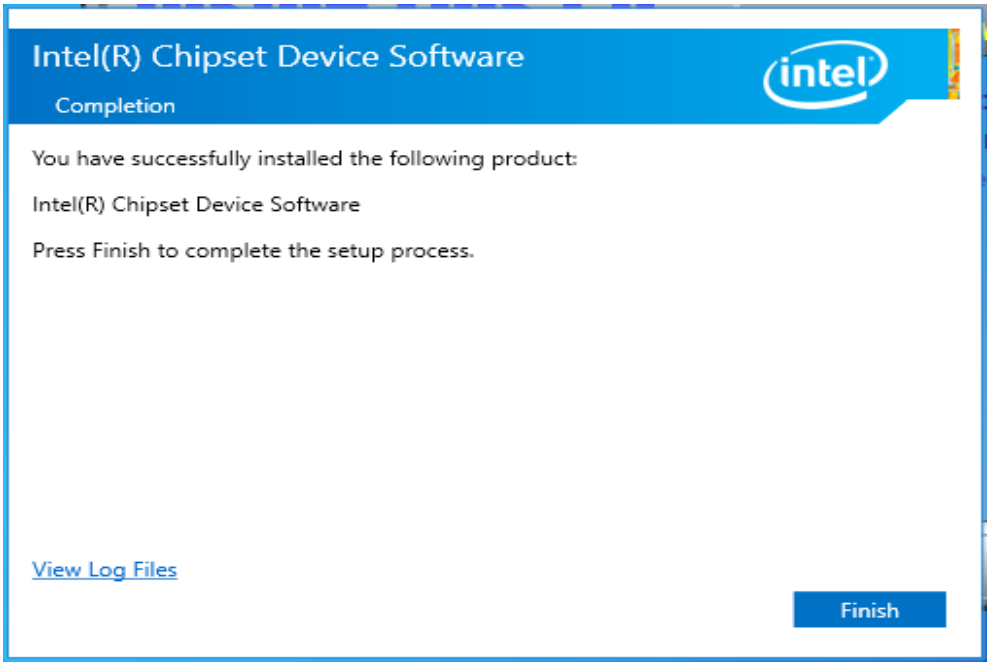
3.2 Intel® Chipset Software Installation Utility

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for the chipset components. Follow the instructions below to complete the installation.

1. Insert the DVD enclosed in the package. Click **Intel** and then **Intel(R) Elkhartlake Chipset Drivers**.

2. Click **Intel(R) Chipset Software Installation Utility**.

3. When the *Welcome* screen to the Intel® Chipset Device Software appears, click **Next** to continue.
4. Click **Yes** to accept the software license agreement and proceed with the installation process.
5. Click **Install** to proceed with the installation process.
6. The driver has been completely installed. Click **Finish** to complete the setup process.



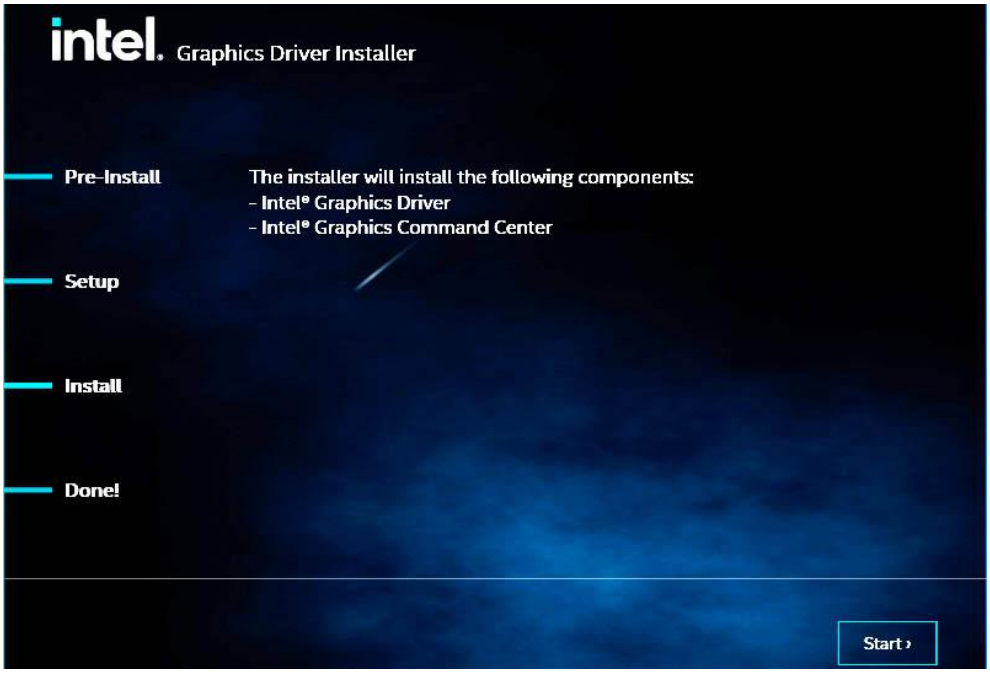
3.3 VGA Driver Installation

1. Click **Intel** and then **Intel(R) Elkhartlake Chipset Drivers**.
2. Click **Intel(R) Elkhartlake Graphics Driver**.

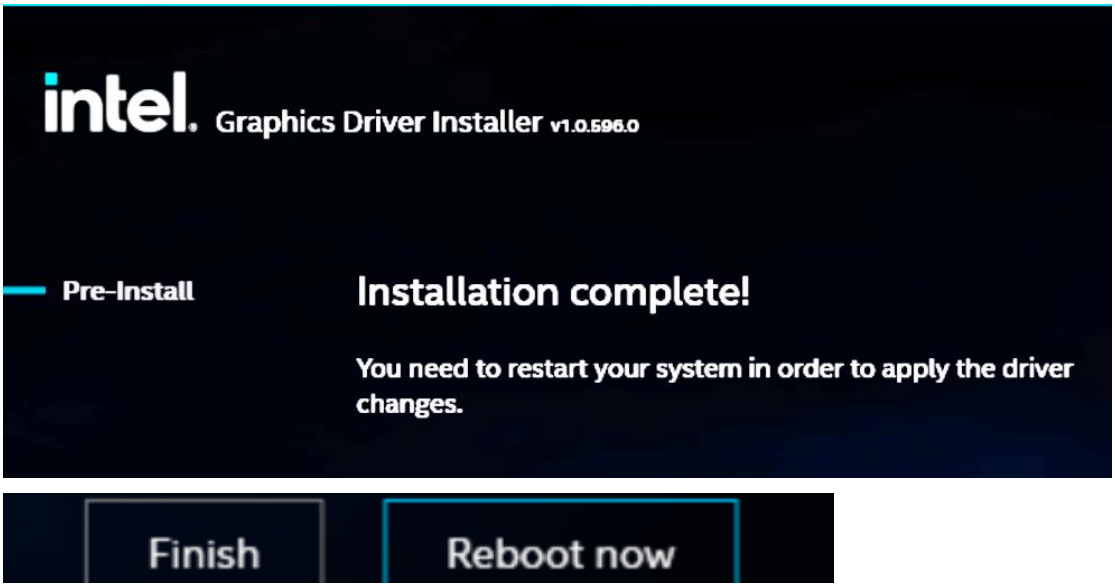
3. Click **Begin Installation** to continue.

4. Click **Yes** to agree with the license agreement.

5. Click **Start**.



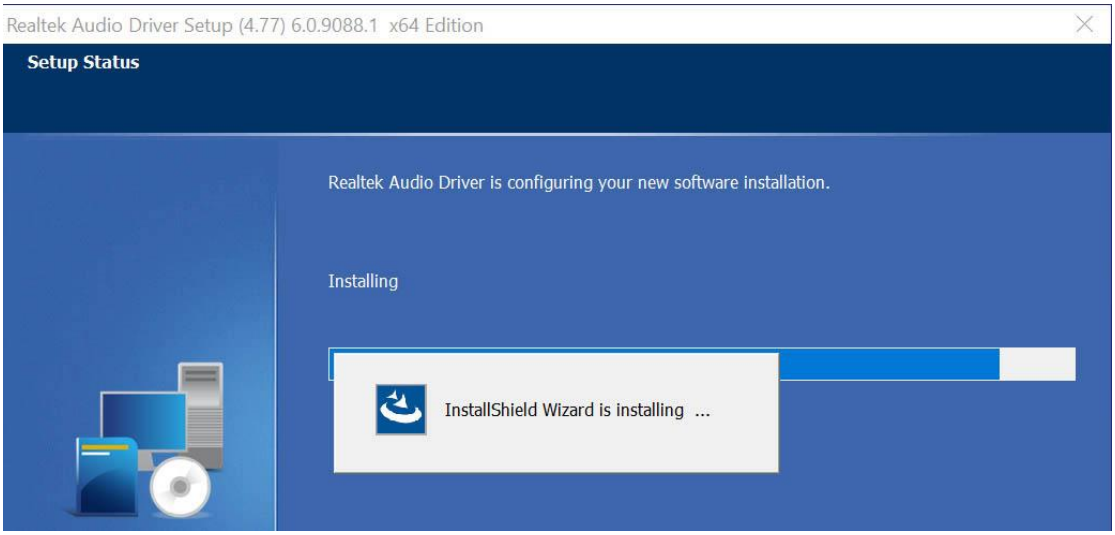
6. When the installation has been completed, click **Finish**.



3.4 HD Audio Driver Installation

1. Click **Intel** and then **Intel(R) Elkhartlake Chipset Drivers**.
2. Click **Realtek High Definition Audio Driver**.

3. On the *Welcome* screen of the InstallShield Wizard, click **Next** to start the installation.

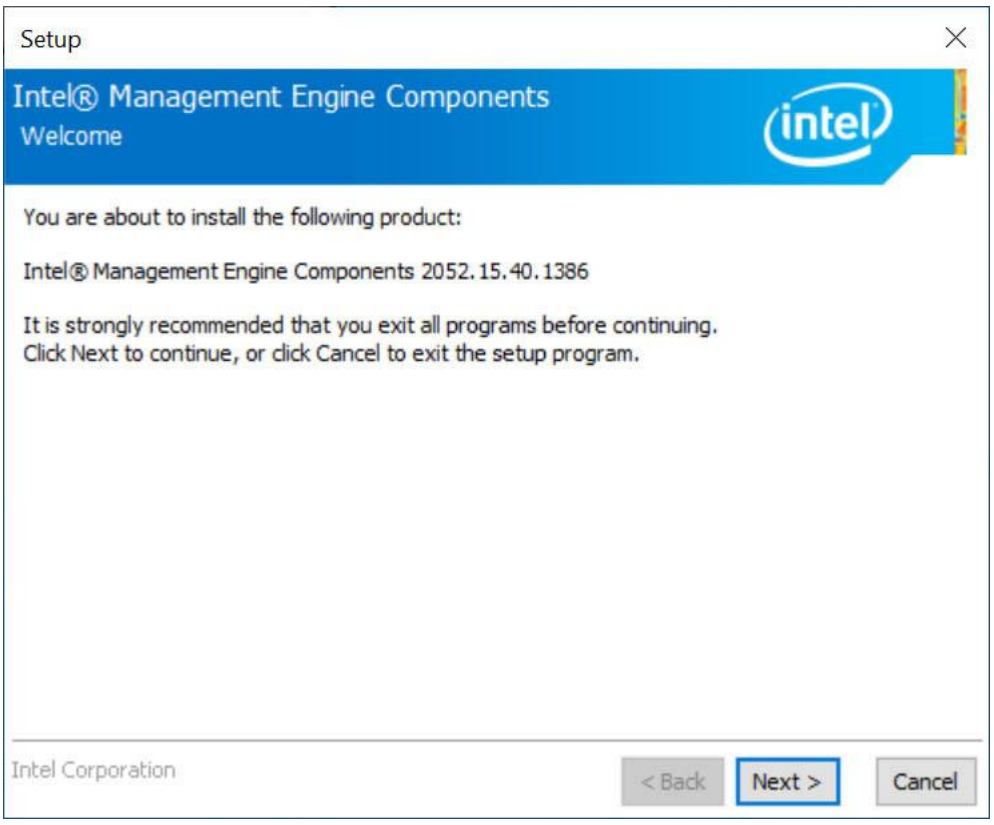


4. When the InstallShield Wizard has finished installing the Realtek Audio Driver, click **Finish**.

3.5 Intel(R) ME Drivers Installation

1. Click **Intel** and then **Intel(R) Elkhartlake Chipset Drivers**.

2. When the Welcome screen to the Intel® Management Engine Components Setup appears, click **Next**.



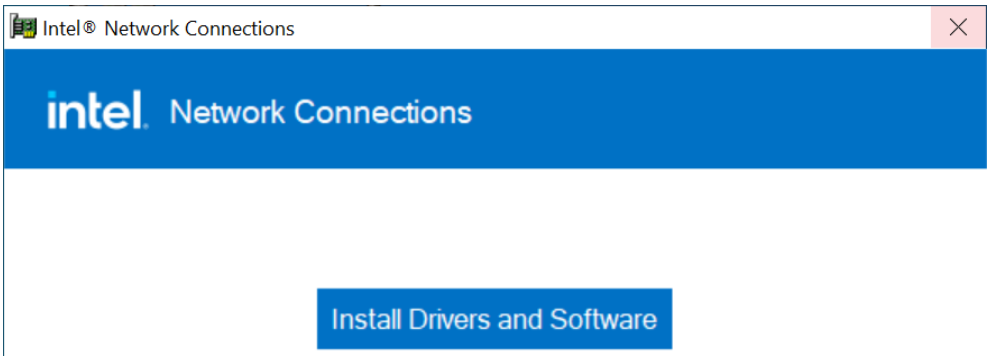
3. Click **Next** to accept the terms in the License Agreement.
4. Click **Next** to install to the default folder, or click Change to choose another destination folder.
5. When you have successfully installed the components, click **Finish**.

3.6 LAN Driver Installation

1. Click **LAN Card** and then **Intel LAN Controller Drivers**.

2. Click **Intel(R) I21x / I22x Gigabit Ethernet Drivers**.

3. On the screen of *Intel® Network Connections*, click **Install Drivers and Software**.



4. In the *Welcome* screen appears, click **Next**.
5. In the *Software License Agreement* screen, click **Next** to accept the terms in the license agreement.
6. In the *Setup Options* screen, click **Next**.
7. The wizard is now ready to begin installation. Click **Install**.
8. In the *Install wizard Completed* screen, click **Finish**.

Chapter 4
BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

- Main Settings
- Advanced Settings
- Chipset Settings
- Security Settings
- Boot Settings
- Save & Exit

4.1 Introduction

The BIOS (Basic Input/Output System) installed in the ROM of your computer system supports Intel® processors. The BIOS provides critical low-level support for standard devices such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

4.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Press the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup.

If you still need to enter Setup, restart the system by pressing the ”Reset” button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again.

The following message will appear on the screen:

```
Press <DEL> to Enter Setup
```

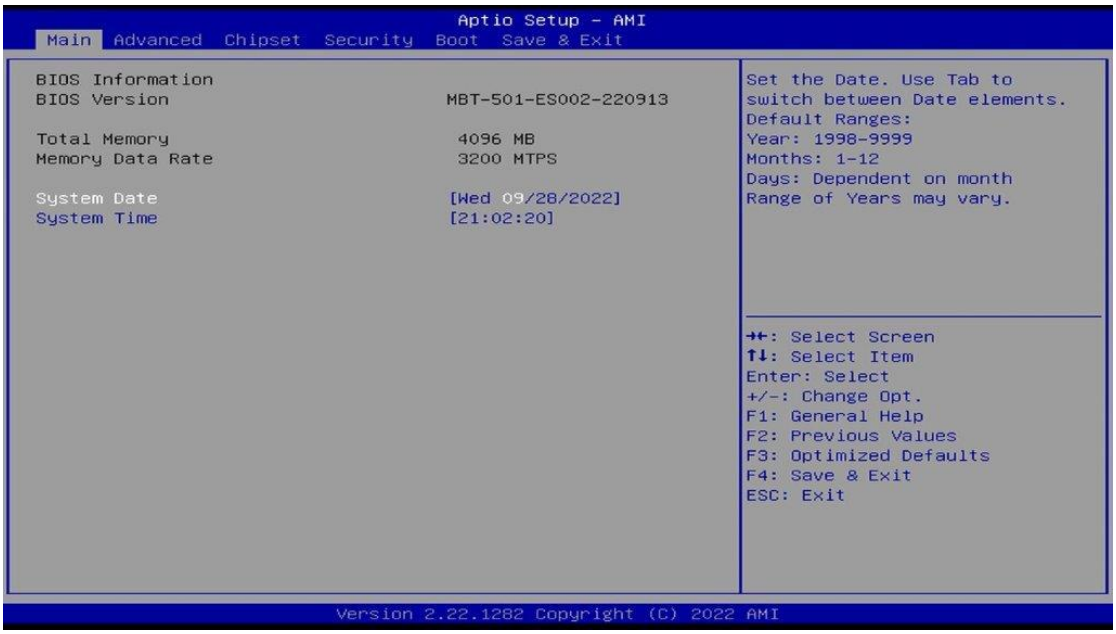
In general, press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help, and <Esc> to quit.

When you enter the BIOS Setup utility, the *Main Menu* screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: It is strongly recommended that you avoid making any changes to the chipset defaults.

These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could make the system unstable and crash in some cases.

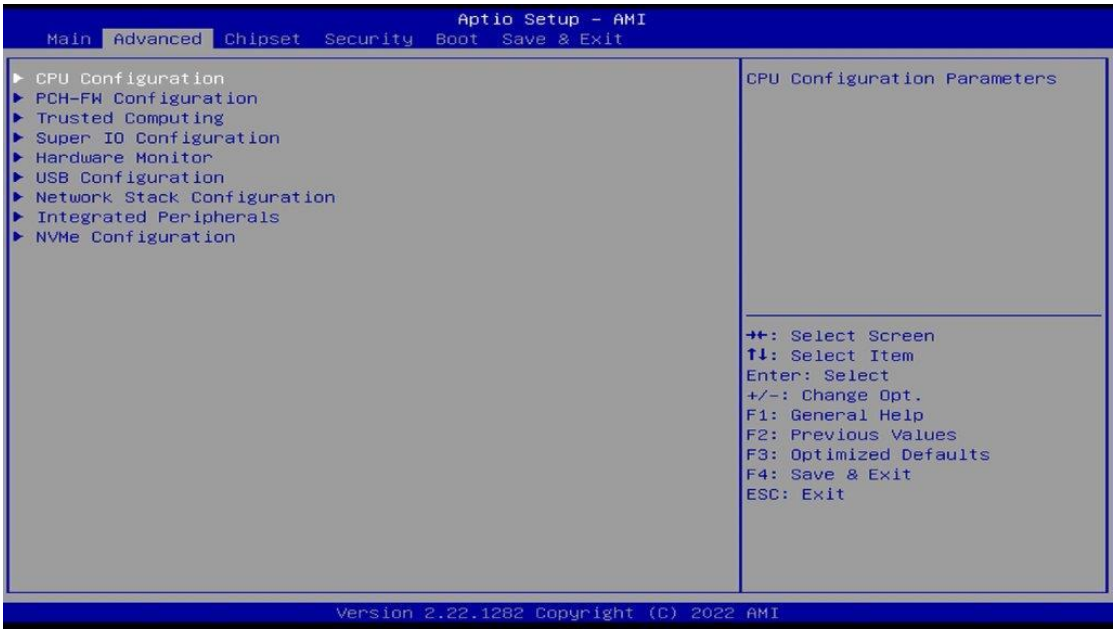
4.3 Main Settings



BIOS Setting	Description
System Date	Sets the date. Use the <Tab> key to switch between the Date elements.
System Time	Set the time. Use the <Tab> key to switch between the Time elements.

4.4 Advanced Settings

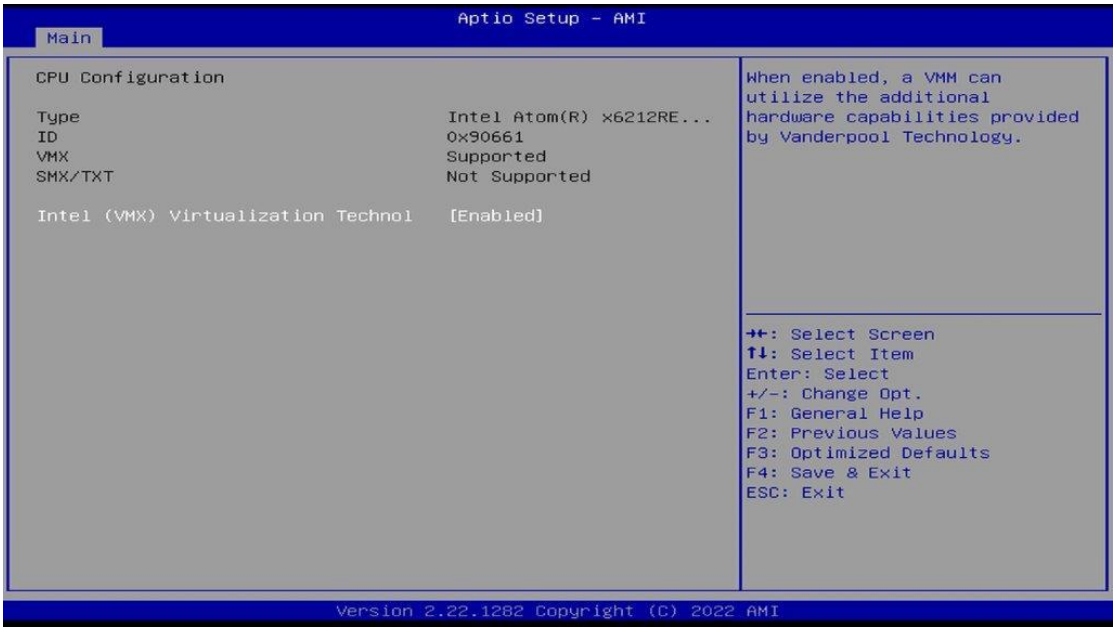
This section allows you to configure, improve your system and allows you to set up some system features according to your preference.

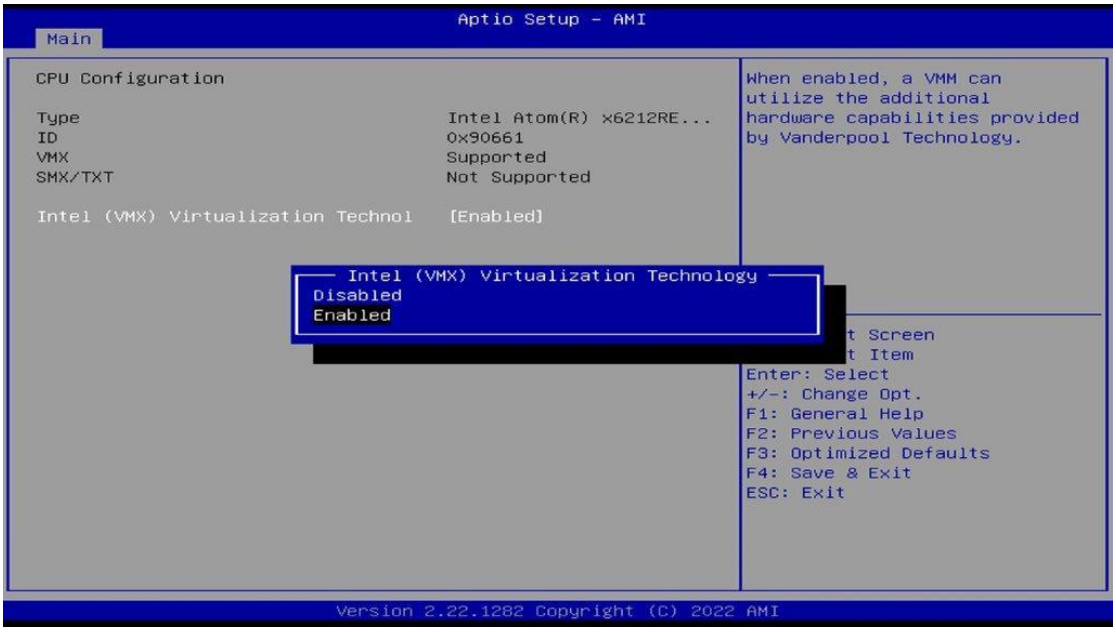


Advanced Settings:

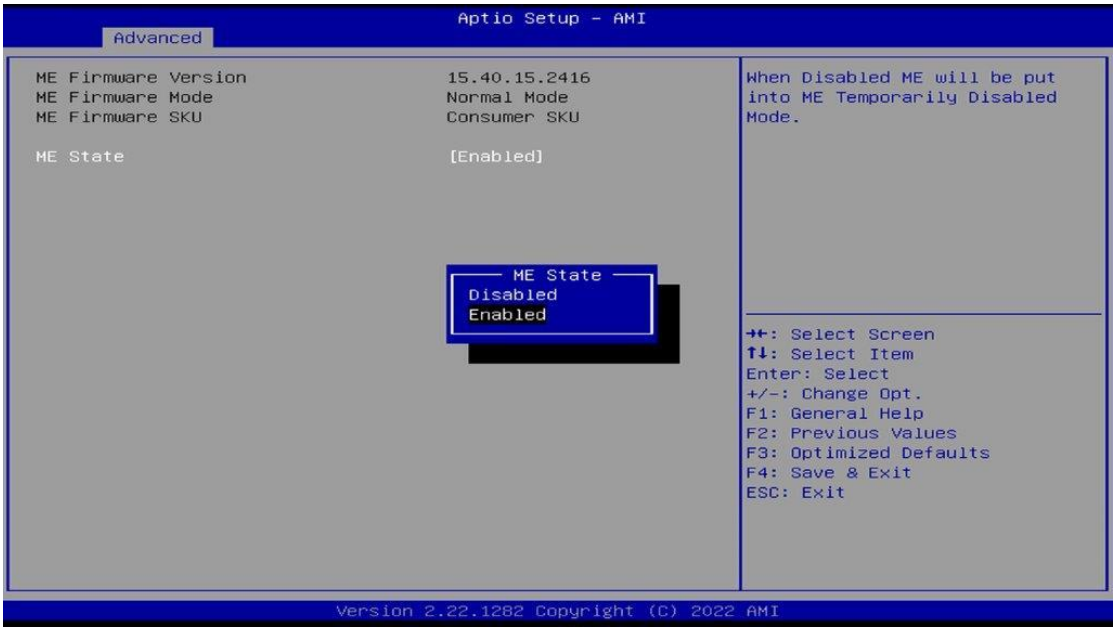
- CPU Configuration
- PCH-FW Configuration
- Trusted Computing
- Super IO Configuration
- Hardware Monitor
- USB Configuration
- Network Stack Configuration
- Integrated Peripherals
- NVMe Configuration

4.4.1 CPU Configuration

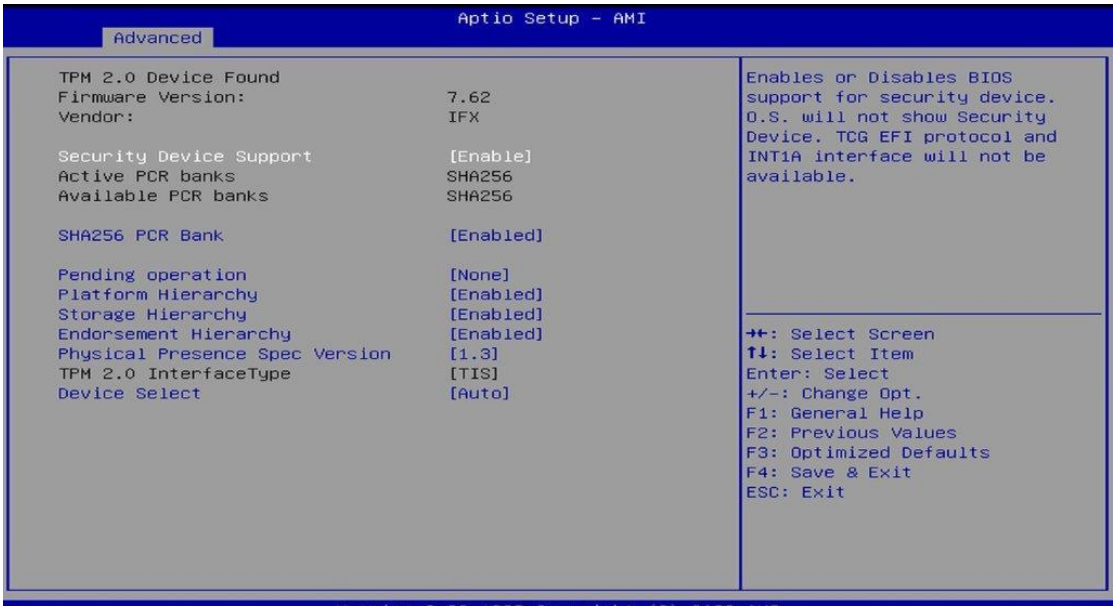




4.4.2 PCH-FW Configuration

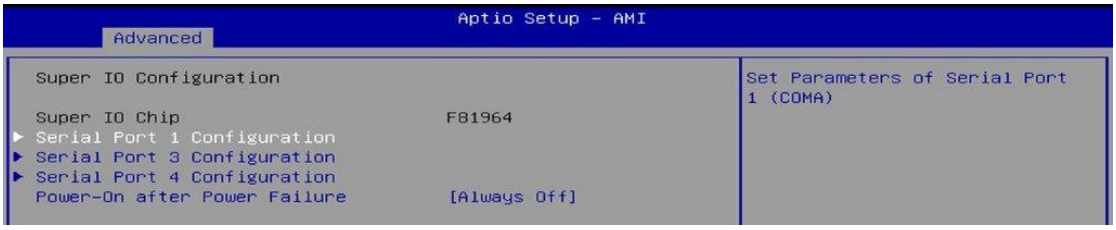


4.4.3 Trusted Computing



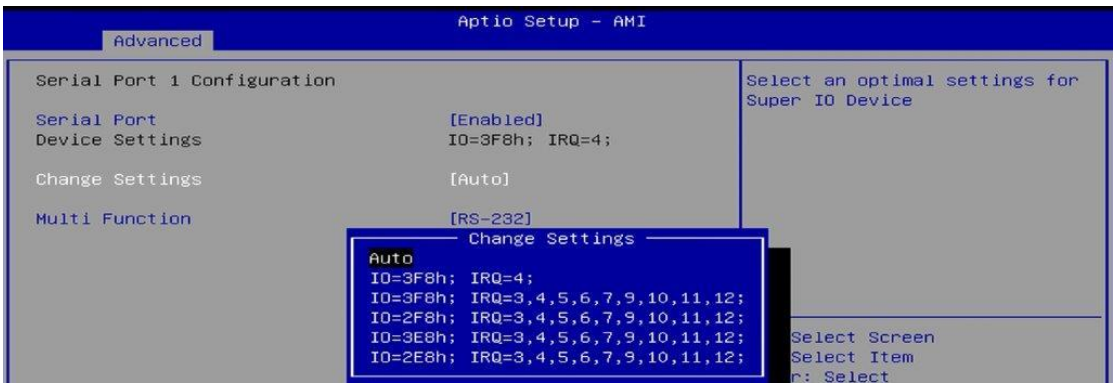
BIOS Setting	Description
Security Device Support	Option: Enable / Disable. OS will not show security device. TCG EFI protocol and INTIA interface will not be available.
SHA256 PCR Bank	Enables / Disables SHA-1 PCR Bank.
Pending operation	Schedule an operation for the security device. Note: Your computer will reboot during restart in order to change state of security device.
Platform Hierarchy	Enables / Disables platform hierarchy.
Storage Hierarchy	Enables / Disables storage hierarchy.
Endorsement Hierarchy	Enables / Disables endorsement hierarchy.
Physical Presence Spec Version	Selects to show the PPI Spec Version (1.2 or 1.3) that the OS supports. **Note:** Some HCK tests might not support 1.3.
Device Select	**TPM 1.2** will restrict support to TPM 1.2 devices only. **TPM 2.0** will restrict support to TPM 2.0 devices only. **Auto** will support both with the default being set to TPM 2.0 deices if not found, and TPM 1.2 device will be enumerated.

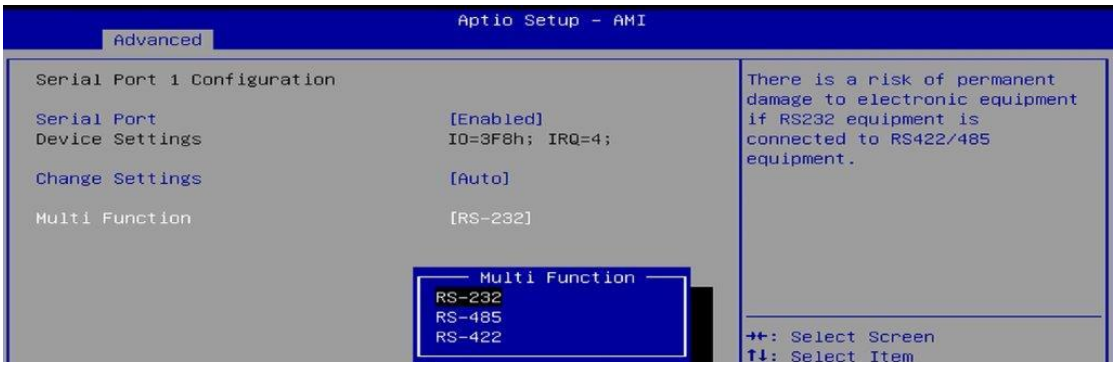
4.4.4 Super IO Configuration



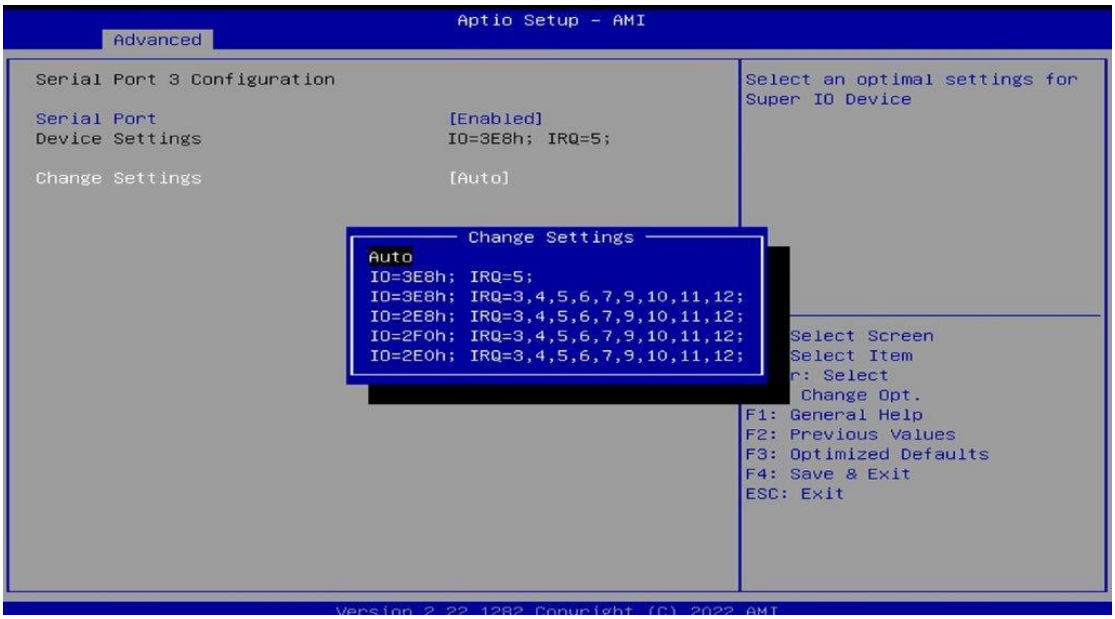
BIOS Setting	Description
Serial Port 1 Configuration	Sets parameters of Serial Port 1 (COMA).
Serial Port 3 Configuration	Sets parameters of Serial Port 3 (COMC).
Serial Port 4 Configuration	Sets parameters of Serial Port 4 (COMD).
Power Failure	The power failure resume control logic of the F81866 is used to recover the system to a pre-defined state after AC power failure.

Serial Port 1 Configuration

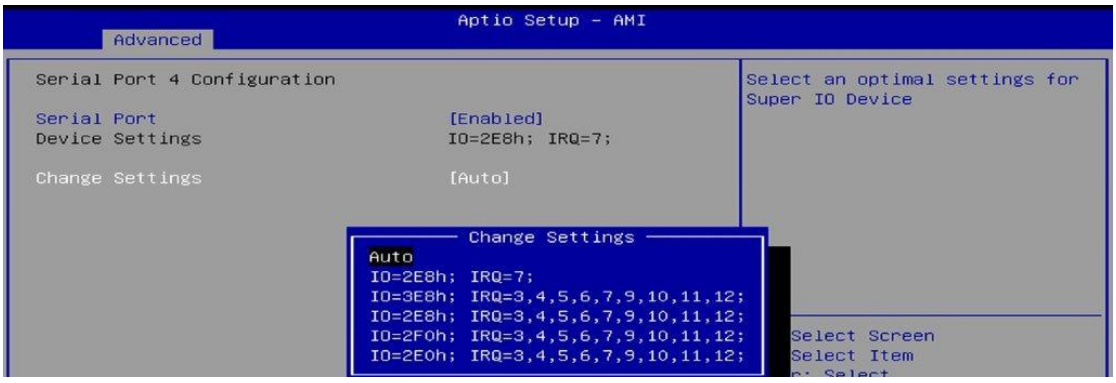




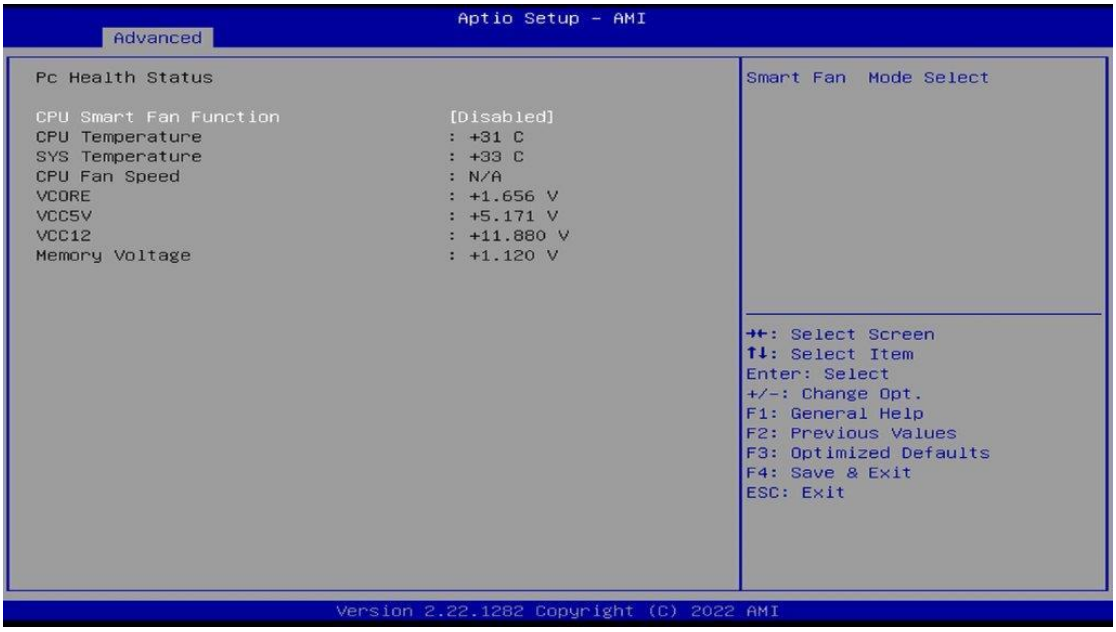
Serial Port 3 Configuration



Serial Port 4 Configuration

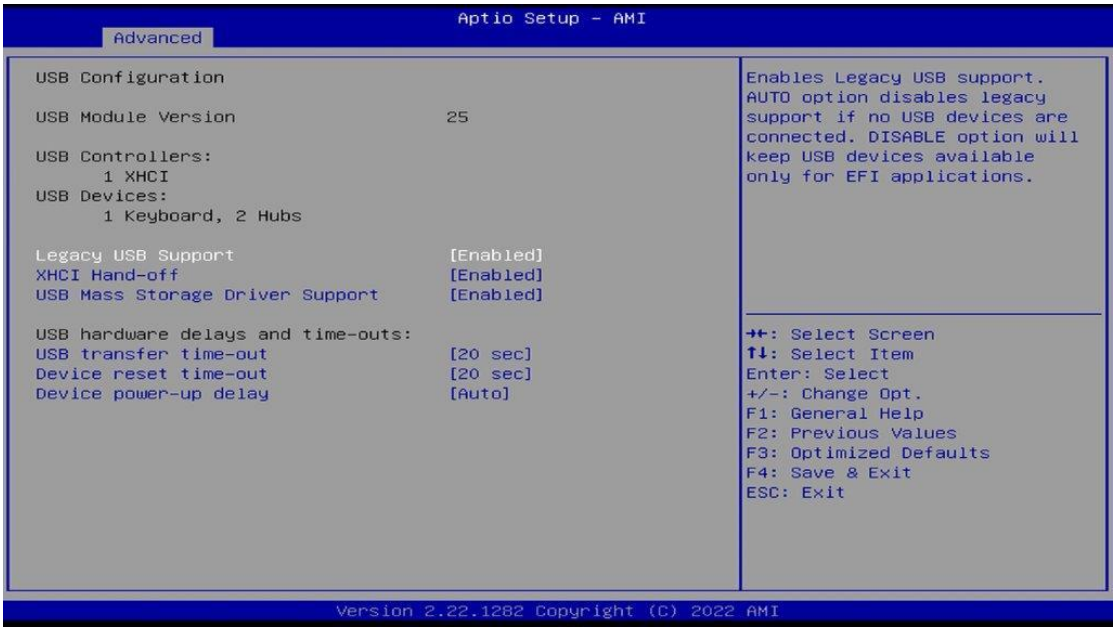


4.4.5 Hardware Monitor



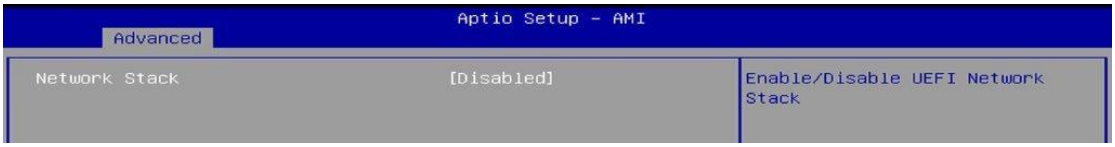
BIOS Setting	Description
Smart Fan Function	This field enables or disables the smart fan feature. Options: Disabled (default), 50 ℃, 60 ℃, 70 ℃, 80 ℃, 90 ℃
Temperatures / Voltages	These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status

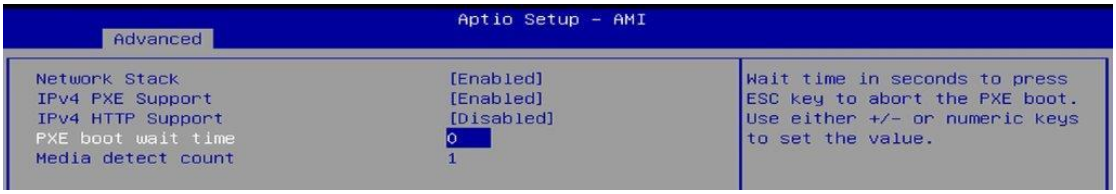
4.4.6 USB Configuration

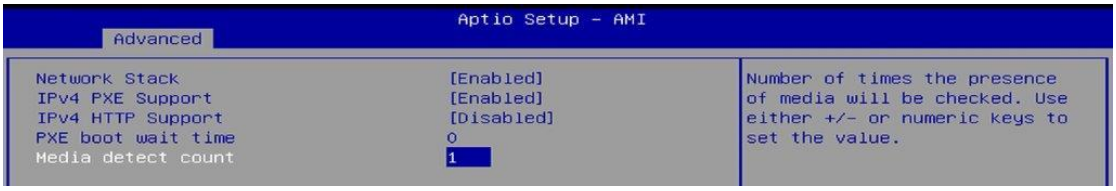


BIOS Setting	Description
Legacy USB Support	• **Enable:** Enables Legacy USB Support. • **Auto:** Disables legacy support if no USB devices are connected. • **Disable:** Keeps USB devices available only for EFI applications.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enables / Disables the support for USB mass storage driver.
USB Transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	Seconds of delaying execution of start unit command to USB mass storage device.
Device power-up delay	The maximum time the device will take before it properly reports itself to the Host Controller. “Auto” uses default value for a Root port it is 100ms. But for a Hub port, the delay is taken from Hub descriptor.

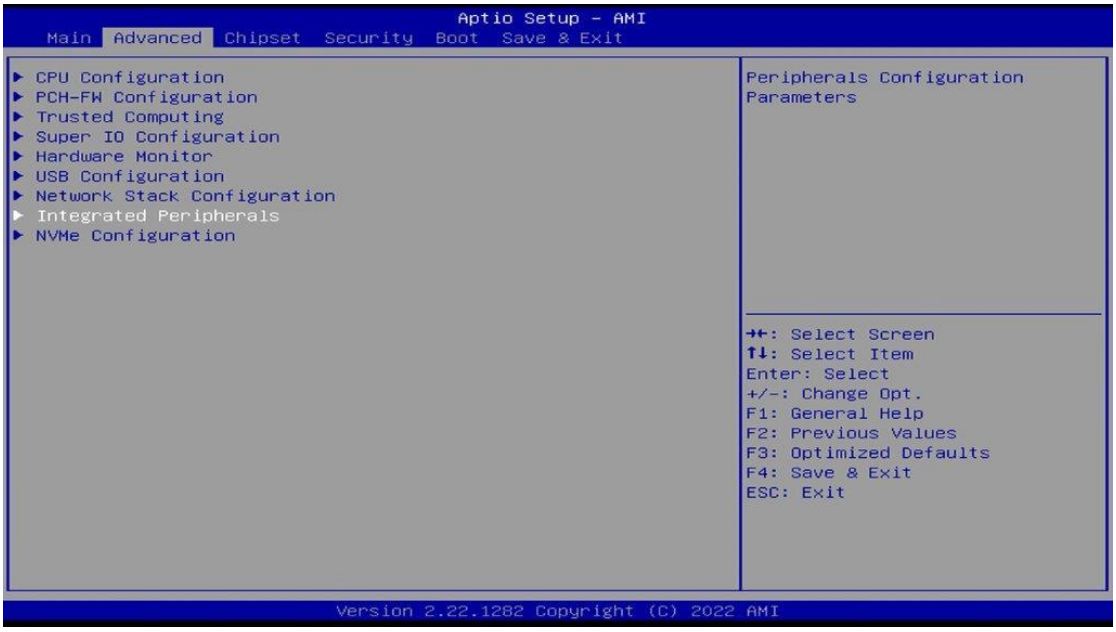
4.4.7 Network Stack Configuration

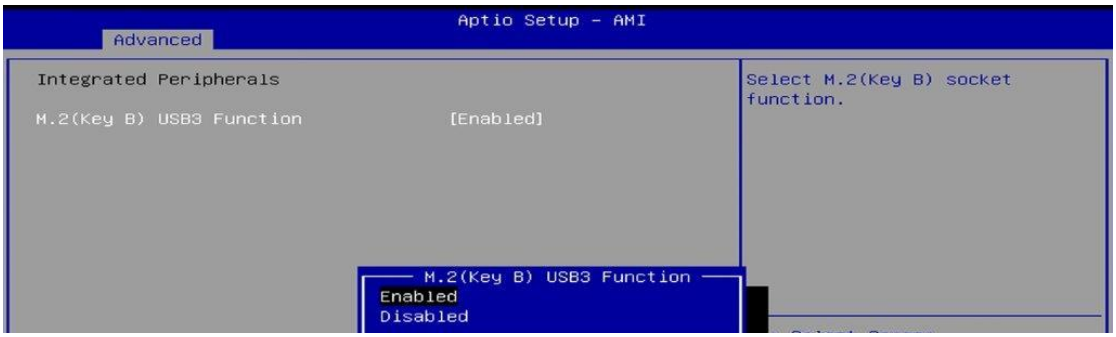




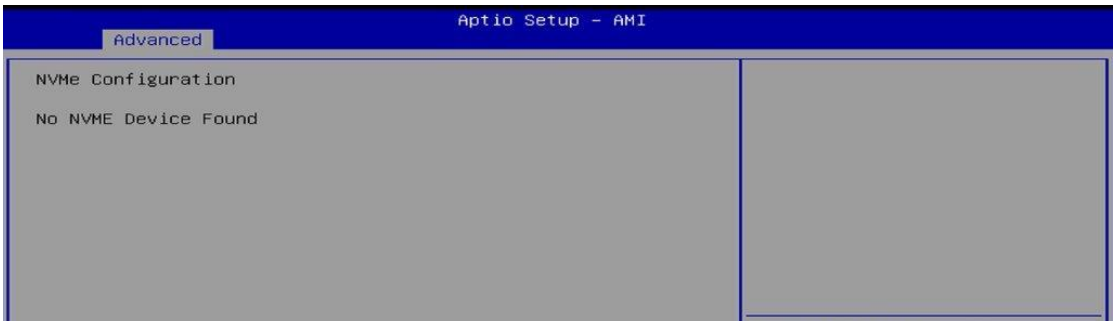


4.4.8 Integrated Peripherals

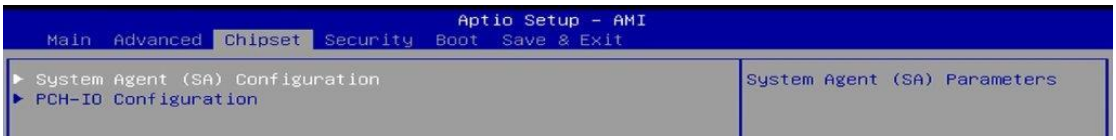




4.4.9 NVMe Configuration



4.5 Chipset Settings



BIOS Setting	Description
System Agent (SA) Configuration	System Agent (SA) parameters
PCH-IO Configuration	PCH parameters

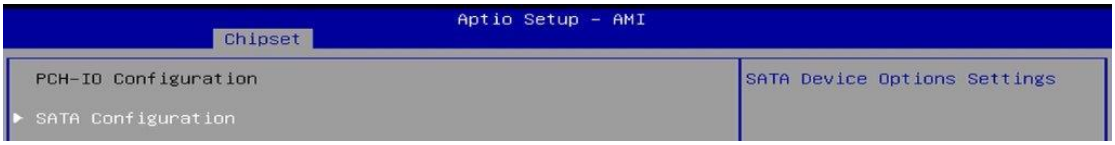
4.5.1 System Agent (SA) Configuration

BIOS Setting	Description
Graphics Configuration	Configures the graphics settings.
VT-d	Checks if VT-d function on MCH is supported.

4.5.1.1. Graphics Configuration

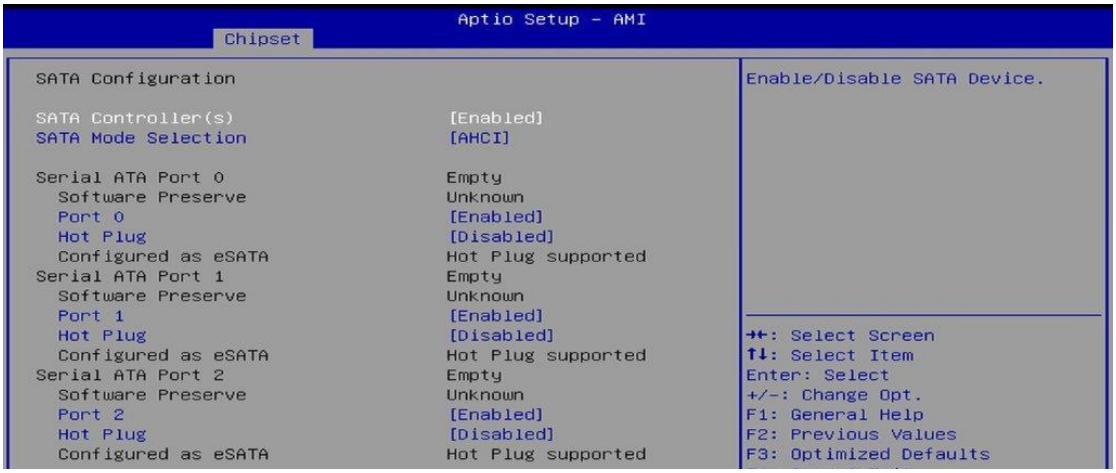
BIOS Setting	Description
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be primary display or select SG for switchable Gfx. Options: Auto, IGFX, PEG, PCI, SG
Internal Graphics	Keep IGFX enabled based on the setup options. Options: Auto, Disabled, Enabled
GTT Size	Sets the GTT size as 2MB, 4MB, or 8MB.
Aperture Size	Sets the aperture size as 128MB, 256MB, 512MB, 1024MB or 2048MB. **Note:** Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048 MB aperture. To use this feature, disable CSM support.

4.5.2 PCH-IO Configuration



BIOS Setting	Description
SATA Configuration	SATA devices options settings

4.5.2.1. SATA Configuration:



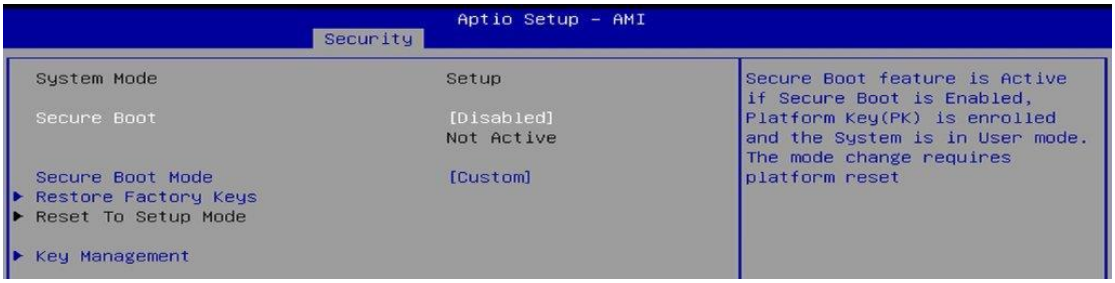
BIOS Setting	Description
SATA Controller(s)	Enables / Disables the SATA device.
SATA Mode Selection	Determines how SATA controller(s) operate. Options: AHCI / Intel RST Premium
Serial ATA Ports	Enables / Disables serial ports.
SATA Ports Hot Plug	Enables / Disables SATA Ports HotPlug.

4.6 Security Settings

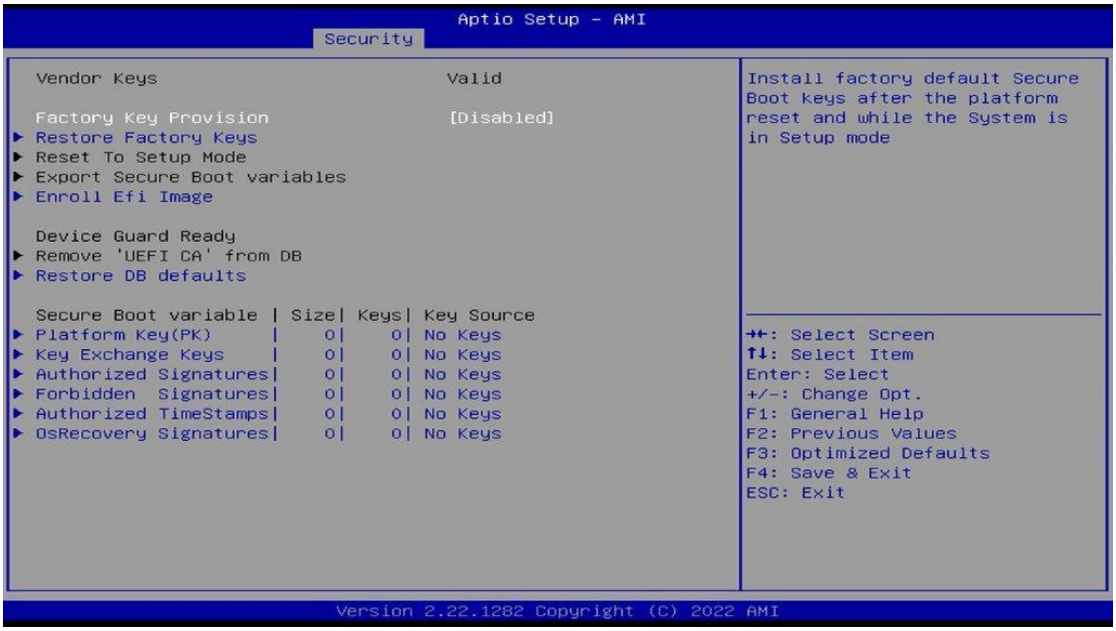
This section allows you to configure, improve your system, and set up some system features according to your preference.

BIOS Setting	Description
Administrator Password	Sets an administrator password for the setup utility.
User Password	Sets a user password.
Secure Boot	Configures Secure Boot.

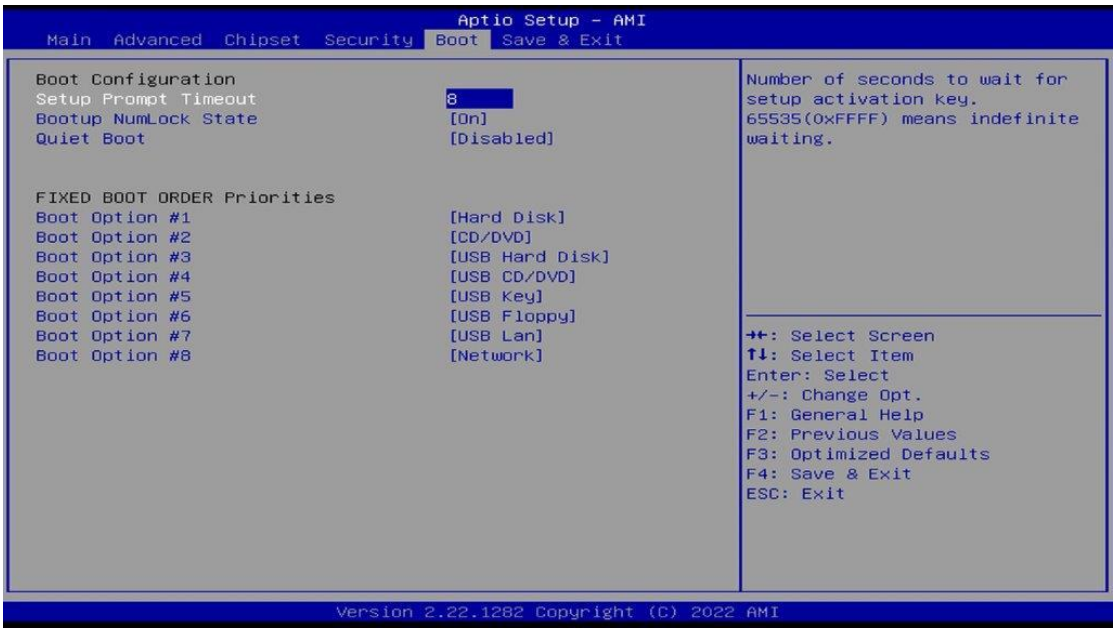
4.6.1 Secure Boot



BIOS Setting	Description
Secure Boot	Secure Boot feature is Active if Secure Boot is enabled. Platform Key (PK) Is enrolled and the system is in User mode. The mode change requires platform reset.
Secure Boot Mode	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.
Restore Factory Keys	Forces system to user mode. Install factory default Secure Boot key databases.
Key Management	Enables expert users to modify Secure Boot Policy variables without full authentication.

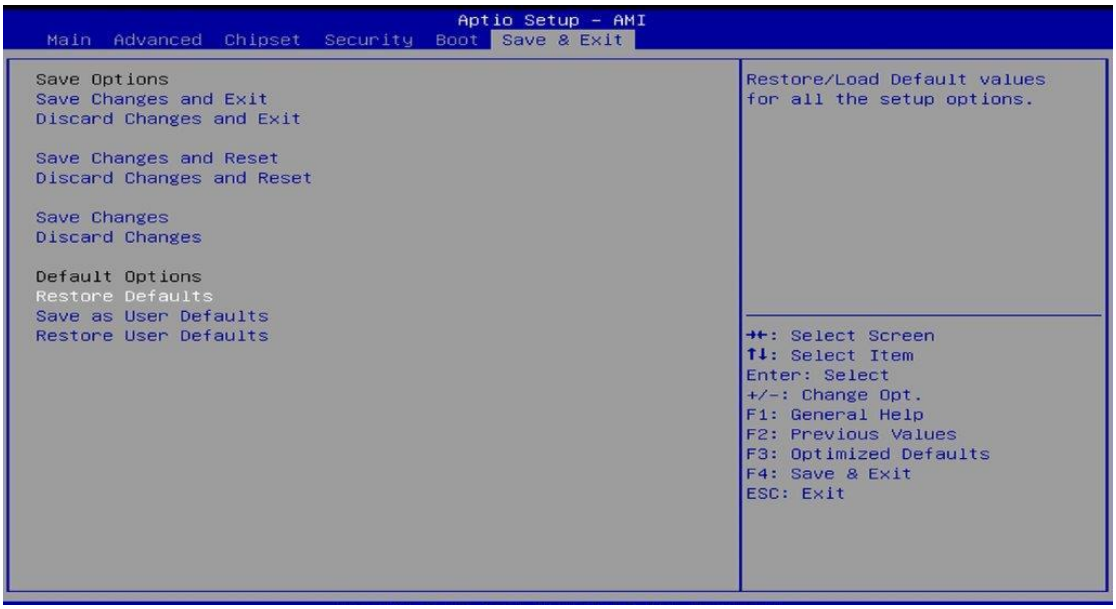


4.7 Boot Settings



BIOS Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Selects the keyboard NumLock state.
Quiet Boot	Enables / Disables Quiet Boot option.
Boot Option Priorities	Sets the system boot order.

4.8 Save & Exit Settings



BIOS Setting	Description
Save Changes and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options.
Restore Defaults	Restores / Loads defaults values for all the setup options.
Save as User Defaults	Saves the changes done so far as user defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

Appendix

This section provides the mapping addresses of peripheral devices and the sample code of watchdog timer configuration.

- I/O Port Address Map
- Interrupt Request Lines (IRQ)
- Watchdog Timer Configuration
- Software Development Kit for WDT.DLL

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A20-0x00000A2F	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x000003F8-0x000003FF	Communications Port (COM1)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x00001800-0x000018FE	Motherboard resources
0x00003090-0x00003097	Standard SATA AHCI Controller
0x00003080-0x00003083	Standard SATA AHCI Controller
0x00003060-0x0000307F	Standard SATA AHCI Controller
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller

Address	Device Description
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x00001854-0x00001857	Motherboard resources
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x0000EFA0-0x0000EFBF	Intel(R) SMBus Controller - 4B23
0x00002000-0x000020FE	Motherboard resources
0x00000060-0x00000060	Standard PS/2 Keyboard
0x00000064-0x00000064	Standard PS/2 Keyboard
0x00003000-0x0000303F	Intel(R) UHD Graphics
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 16	High Definition Audio Controller
IRQ 4294967288~90	Intel(R) Ethernet Controller (3) I225-IT
IRQ 4	Communications Port (COM1)
IRQ 5	Communications Port (COM3)
IRQ 7	Communications Port (COM4)
IRQ 4294967287	Intel(R) Ethernet Controller (3) I225-IT #2
IRQ 4294967286	Intel(R) Ethernet Controller (3) I225-IT #2
IRQ 4294967285	Intel(R) Ethernet Controller (3) I225-IT #2
IRQ 4294967294	Standard SATA AHCI Controller
IRQ 4294967293	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 55~204	Microsoft ACPI-Compliant System
IRQ 256~511	Microsoft ACPI-Compliant System
IRQ 1	Standard PS/2 Keyboard
IRQ 12	Microsoft PS/2 Mouse
IRQ 4294967284	Intel(R) Ethernet Controller (3) I225-IT #3
IRQ 4294967283	Intel(R) Ethernet Controller (3) I225-IT #3
IRQ 4294967282	Intel(R) Ethernet Controller (3) I225-IT #3
IRQ 4294967291	Intel(R) Management Engine Interface #1
IRQ 4294967292	Intel(R) UHD Graphics
IRQ 0	System timer

C. Watchdog Timer Configuration

The Watchdog Timer (WDT) is used to generate a variety of output signals after a user programmable count. The WDT is suitable for the use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven.

Under normal circumstance, you will need to restart the WDT at regular intervals before the timer counts to zero.

Sample Code:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]); void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
unsigned char bBuf; unsigned char bTime; char **endptr;

char SIO;
printf("Fintek 81866 watch dog program\n"); SIO = Init_F81866();
if (SIO == 0)
{
printf("Can not detect Fintek 81866, program abort.\n"); return(1);
}//if (SIO == 0)

if (argc != 2)
{
printf(" Parameter incorrect!!\n"); return (1);
}

bTime = strtol (argv[1], endptr, 10);
printf("System will reset after %d seconds\n", bTime);

if (bTime)
{       EnableWDT(bTime);   } else
{       DisableWDT();   } return 0;
```

```
}
//-----------------------------------------------------------------------------
void EnableWDT(int interval)
{
unsigned char bBuf;

bBuf = Get_F81866_Reg(0x2B);  bBuf &= (~0x20);
Set_F81866_Reg(0x2B, bBuf);    //Enable WDTO

Set_F81866_LD(0x07);       //switch to logic device 7
Set_F81866_Reg(0x30, 0x01);    //enable timer

bBuf = Get_F81866_Reg(0xF5);  bBuf &= (~0x0F);
bBuf |= 0x52;
Set_F81866_Reg(0xF5, bBuf);            //count mode is second  Set_F81866_Reg(0xF6,
interval);    //set timer
bBuf = Get_F81866_Reg(0xFA);  bBuf |= 0x01;
Set_F81866_Reg(0xFA, bBuf);    //enable WDTO output

bBuf = Get_F81866_Reg(0xF5);  bBuf |= 0x20;
Set_F81866_Reg(0xF5, bBuf);    //start counting
}
//-----------------------------------------------------------------------------
void DisableWDT(void)
{
unsigned char bBuf;
Set_F81866_LD(0x07);       //switch to logic device 7  bBuf = Get_F81866_Reg(0xFA);
bBuf &= ~0x01;
Set_F81866_Reg(0xFA, bBuf);    //disable WDTO output

bBuf = Get_F81866_Reg(0xF5);  bBuf &= ~0x20;
bBuf |= 0x40;
Set_F81866_Reg(0xF5, bBuf);    //disable WDT
}
//-----------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81866_BASE; void Unlock_F81866 (void); void Lock_F81866 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81866(void)
{
unsigned int result; unsigned char ucDid;

F81866_BASE = 0x4E;
result = F81866_BASE;

ucDid = Get_F81866_Reg(0x20);
if (ucDid == 0x07)      //Fintek 81866
{       goto Init_Finish; }

F81866_BASE = 0x2E;
result = F81866_BASE;

ucDid = Get_F81866_Reg(0x20);
if (ucDid == 0x07)      //Fintek 81866
{       goto Init_Finish; }

F81866_BASE = 0x00;
result = F81866_BASE;

Init_Finish:
return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81866 (void)
{
outportb(F81866_INDEX_PORT, F81866_UNLOCK); outportb(F81866_INDEX_PORT,
F81866_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81866 (void)
{
outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
Unlock_F81866();
outportb(F81866_INDEX_PORT, F81866_REG_LD);
outportb(F81866_DATA_PORT, LD);  Lock_F81866();
```

```
}
//---------------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
Unlock_F81866(); outportb(F81866_INDEX_PORT, REG); outportb(F81866_DATA_PORT,
DATA); Lock_F81866();
}
//---------------------------------------------------------------------------
unsigned char Get_F81866_Reg(unsigned char REG)
{
unsigned char Result; Unlock_F81866();
outportb(F81866_INDEX_PORT, REG); Result = inportb(F81866_DATA_PORT);
Lock_F81866();
return Result;
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef       F81866_H
#define        F81866_H     1
//---------------------------------------------------------------------------
#defineF81866_INDEX_PORT   (F81866_BASE)
#defineF81866_DATA_PORT    (F81866_BASE+1)
//---------------------------------------------------------------------------
#defineF81866_REG_LD   0x07
//---------------------------------------------------------------------------
#define F81866_UNLOCK  0x87
#defineF81866_LOCK       0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char); unsigned char
Get_F81866_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif //      F81866_H
```

D. Software Development Kit for WDT.DLL

1. OS Supported

Windows SP (32-bit / 64-bit) or above

2. Driver Installation

- **For 32-bit environment:**

  Step 1:
  Copy the file **KMUI32_1K.SYS** to <%WINDIR%>\SYSTEM32\DRIVERS.

  Step 2:
  The following parameters must be written to your registry.

  HKLM,"System\CurrentControlSet\Services\KMUI32_1K","ErrorCo
  ntrol",%REG_DWORD%,0x00000001

  HKLM,"System\CurrentControlSet\Services\
  KMUI32_1K","Type",%REG_DWORD%,0x00000001

  HKLM,"System\CurrentControlSet\Services\
  KMUI32_1K","Start",%REG_DWORD%,0x00000000

  HKLM,"System\CurrentControlSet\Services\
  KMUI32_1K","DisplayName",%REG_SZ%,"KMUI32_1K"

  Step 3:
  Restart the system.

- **For 64-bit environment:**

  Step 1:
  Copy “KMUI64_1K.SYS” file to <%WINDIR%>\SYSTEM32\DRIVERS

  Step 2:
  The following parameters must be written to your registry.

  HKLM,"System\CurrentControlSet\Services\KMUI64_1K","ErrorControl",
  %REG_DWORD%,0x00000001

  HKLM,"System\CurrentControlSet\Services\
  KMUI64_1K","Type",%REG_DWORD%,0x00000001

  HKLM,"System\CurrentControlSet\Services\
  KMUI64_1K","Start",%REG_DWORD%,0x00000000

  HKLM,"System\CurrentControlSet\Services\
  KMUI64_1K","DisplayName",%REG_SZ%,"KMUI64_1K"

  Step 3:
  Restart the system.

Note: Do not install both of the 32-bit and 64-bit drivers on an operating system.

---

3. Exportion from IB_WDT.DLL / IB_WDT.64.DLL

```
extern "C" __declspec(dllexport) int __stdcall InstallDriver(void);
extern "C" __declspec(dllexport) int __stdcall RemoveDriver(void);
extern "C" __declspec(dllexport) char* __stdcall GetWDTInfo(void);
extern "C" __declspec(dllexport) int __stdcall EnableWDT(int);
extern "C" __declspec(dllexport) int __stdcall DisableWDT(int);
extern "C" __declspec(dllexport) int __stdcall IsDioAvailable(int);
extern "C" __declspec(dllexport) int __stdcall SetDioInputMask(int);
extern "C" __declspec(dllexport) int __stdcall SetDioOutputMask(int);
extern "C" __declspec(dllexport) int __stdcall GetDioInput(int);
extern "C" __declspec(dllexport) int __stdcall SetDioOutput(int);
```

Note:

1. The **IB_WDT.DLL** is of 32-bit and works on 32-bit and 64-bit Windows operating system. The “IB_WDT.64.DLL” is for 64bit Windows only.
2. The routines are not thread-safe. Your software engineers should take the responsibility to avoid multi-entry condition.

- **Driver Initialization & Deinitalization**

```
extern "C" __declspec(dllexport) int __stdcall InstallDriver(void);
```

Input : None

Output : Return 1 if device driver loads successfully; otherwise return 0.

Note: This function should be invoked before Watchdog and Digital I/O routines.

```
extern "C" __declspec(dllexport) int __stdcall RemoveDriver(void);
```

Input : None

Output : Always return 1.

Note: This function should be invoked before the program closes and it will release the device driver and memory for **ib_wdt.dll**. If the program is closed without calling this routine, resource leak may occur.

- **Watchdog**

extern "C" __declspec(dllexport) char * __stdcall GetWDTInfo(void);

Input : None
Output : Return a string that describes the module information.

extern "C" __declspec(dllexport) int __stdcall EnableWDT(int);

Input : Timer interval, depending on the WDT chip
Output : Always return “0”

For further information, refer to the datasheet for WDT or contact your sales representative.

extern "C" __declspec(dllexport) int __stdcall DisableWDT(int);

Input : Dummy data and will be ignored.
Output : Always return “0”

- **Digital I/O**

extern "C" __declspec(dllexport) int __stdcall IsDioAvailable(int);

Input : Dummy data and will be ignored

Output : Return 1 if the digital I/O is available, otherwise return 0.

extern "C" __declspec(dllexport) int __stdcall SetDioInputMask(int);

Input: : Hardware parameter for digital I/O input function call.

For example, the 6 GPIO functions:

GPIO_0 to GPIO_2 are mapped as the input functions, and GPIO_4 to GPIO_6 are mapped as the output functions.

In this case, the parameter for “SetDioInputMask” is 0x07 and it indicates that GPIO_0 to GPIO_2 are the input functions.

The parameter for “SetDioOutputMask” is 0x70 and it indicates that GPIO_4 to GPIO_6 are the output functions.

Output : Dummy data and should be ignored.

extern "C" __declspec(dllexport) int __stdcall SetDioOutputMask(int);

Input : Hardware parameter for digital I/O output function call

For further information, refer to the following explanation of “SetDioInputMask” routine.

SetDioInputMask:

```
if ((*lpIsDioAvailable)(0))
        {
                int DioInput;
                printf(" Test for digital IO ....\n");

                //Please check digital IO setting in BIOS setup utility
                //Here example as follow:
                //    Digital GPIO [1..3] = Input
                //    Digital GPIO [4..6] = Output

                //set hardware information for GPIO chip
                //bit 0..2 : input for GPIO_0 to GPIO_2
                //bit 4..6 : output for GPIO_4 to GPIO_6
               (*lpSetDioInputMask)(0x07);
               (*lpSetDioOutputMask)(0x70);

                DioInput = (*lpGetDioInput)(0);
                printf(" Current GPIO_0 to GPIO_2 is 0x%X\n", DioInput);

      while(1)
      {
                          (*lpSetDioOutput)(0x00);
                            printf(" Set GPIO_4 to GPIO_6 to LOW\n");
                          (*lpSetDioOutput)(0x70);
                            printf(" Set GPIO_4 to GPIO_6 to HIGH\n");
                          (*lpSetDioOutput)(0x30);
                            printf(" Set GPIO_4 to GPIO_5 to HIGH\n");
                          (*lpSetDioOutput)(0x60);
                            printf(" Set GPIO_5 to GPIO_6 to HIGH\n");

                            Sleep(500);
                            if (_kbhit())
                            {
                break;
        }//if (kbhit())
                }//while(1)
        }//if ((*lpIsDioAvailable)(0))
```

Note: Be sure to set up the input / output for GPIO bits in BIOS identically with the GPIO hardware information above.

E. Motherboard MCU ISP Specifications

1. Description

Security MCU provides following functionality

- **Getting Firmware Version**
  Software can get the firmware version, MCU provides commands to get current Major Version, Minor version and build version.

- **Setting Power-On-Delay Timer**
  MCU provides command to set power on delay timer, when arrived the setting time, MCU will send power button to let the system power on.

- **Setting Power-Off-Delay Timer**
  MCU provides command to set power off delay timer, when arrived the setting time, MCU will send power button to let the system power off.

- **Getting Status**
  MCU provides command to get current status which includes the power on delay timer setting value and power off delay timer setting value.

Note: Before using the ISP, your software engineer has to make sure the firmware version (GET_FORMWARE_VERSION) MUST be as follows to make the ISP function workable.

Major version is 0.

Minor version is 0.

Build version is 1 (or above).

---

2. Protocol

- **Signal transmit format**

Bandwidth
Baud rate: 19200 bps

Data Format
Parity: No Parity
1 start bit
8 data bits
1 stop bit

- **Packet Format**

Header	Size	Command	Data	CRC
2 bytes	1 byte	1 byte	0 – 64 bytes	2 bytes

Header bytes indicate start of the packet.

Size specifies number of bytes for data field.

Command identifies action, which is required to be performed on the data.

CRC verifies data integrity for header, size, command and data bytes.

- **CRC**

Protocol uses 16-bit CCITT CRC to verify data integrity.
$P(x) = X^{16}+X^{12}+X^{5}+1$

```
unsigned calc_crc(unsigned char *data, unsigned n, unsigned start) {
	unsigned I, k, q, c, crcval;
	crcval=start;
	for (I=0; I<n; I++) {
		c=data(I) & 0xFF;
		q=(crcval^c) & 0x0F;
		crcval=(crcval>>4)^(q*0x1081);
		q=(crcval^(c>>4)) & 0x0F;
		crcval=(crcval>>4)^(q*0x1081);
	}
	return crcval;
}
```

- **Communications flow**

  Communication between PC and Security MCU utilizes Master-Slave model, where PC is a master, and Security MCU is a slave. Master sends requests to the slave, and slave has to reply to them. Slave acts like a passive device and cannot send any requests to the master.

3. Command and Reply Codes

- **Summary**

Code	Value	Description
GET_FIRMWARE_VERSION	0x01	Get Firmware version
SET_POWER_ON_DELAY_TIMER	0x04	Power on delay timer setting
SET_POWER_OFF_DELAY_TIMER	0x05	Power off delay timer setting
GET_STATUS	0x10	Get Current Status

- **Getting Firmware Version**

  Parameter: GET_FIRMWARE_VERSION

  Reads version number of the security MCU firmware.

  Request:

Header	Size	Command	Data	CRC
0xFF 0xEE	0x00	GET_FIRMWARE_VERSION	None	

  Reply:

Header	Size	Command	Data	CRC
0xFF 0xEE	Size of Version structure	GET_FIRMWARE_VERSION	BSL Version Structure	

  BSL Version Structure

Field	Type	Description
Major Version	Byte	Major version number
Minor Version	Byte	Minor version number
Build	Byte	Build version number

- **Setting Power-On Delay Timer**

  Parameter: SET_POWER_ON_DELAY_TIMER

  Sets power on delay timer.

  Request:

Header	Size	Command	Data0	Data1	CRC
0xFF 0xEE	0x02	SET_POWER_ON_DELAY_TIMER	N (mins)	N (secs)	

  Reply

Header	Size	Command	Data	CRC
0xFF 0xEE	0x00	SET_POWER_ON_DELAY_TIMER	None	

- **Setting Power-Off Delay Timer**

  Parameter: SET_POWER_OFF_DELAY_TIMER

  Sets power off delay timer.

  Request:

Header	Size	Command	Data0	Data1	CRC
0xFF 0xEE	0x02	SET_POWER_OFF_DELAY_TIMER	N (mins)	N (secs)	

  Reply

Header	Size	Command	Data	CRC
0xFF 0xEE	0x00	SET_POWER_OFF_DELAY_TIMER	None	

- **Getting Status**

  Gets the power-on-delay timer and power-off-delay timer.

  Request:

Header	Size	Command	Data	CRC
0xFF 0xEE	0x00	GET_STATUS	None	

  Reply:

Header	Size	Command	Data	CRC
0xFF 0xEE	0x04	GET_STATUS	Status structure	

  BSL Version Structure

Field	Type	Description
Power on delay timer	Word	Byte4+ Byte5
Power off delay timer	Word	Byte6+ Byte7